Enhanced Silicon Crystallization on Dielectric Materials at Reduced Temperature

Kangjian Cheng, Jingyan Huang, and Wen Siang Lew, *Senior Member, IEEE*

***Abstract*— We report the demonstration of the crystallization of amorphous arsenic and boron-doped silicon films on dielectric substrates at reduced thermal budgets. The conventional methods to form polycrystalline silicon generally require growth temperatures of at least 600 °C, or high-temperature post-annealing to transform the silicon structure from amorphous into polycrystalline. Here, we show the formation of high-quality polycrystalline silicon at temperatures between 500 °C and 550 °C, which helps to reduce the thermal budget strain on heterojunction bipolar transistor devices. This advancement is attained by selecting buffer layer materials and fine-tuning film thickness. A notable increase in the film conductivity was observed, with improvements of 66% and 1719% for arsenic and boron-doped silicon films, respectively, compared to structured-mixed silicon films. The crystalline nature of the films is confirmed through top-view scanning electron microscopy coupled with ImageJ software analysis, offering a rapid, inline approach for crystal percentage quantification. Additionally, cross-sectional transmission electron microscopy analyses verify the complete film crystallization.**

***Index Terms*—Crystalline area fraction, Front-End-of-Line (FEOL), Heterojunction Bipolar Transistor (HBT), Low temperature polysilicon (LTPS), Microcrystalline silicon**

I. INTRODUCTION

THE demand for faster processing devices possesses new challenges for the development of heterojunction bipolar transistors (HBT). One critical requirement is achieving a thinner base layer W_B to enhance the current amplifying ratio β and reduce the base transit time τ_B, leading to a faster and more efficient device.

$$\beta = \frac{\mu_{nB} L_{pE} N_{NE}^{+}}{\mu_{pE} W_B N_{PB}^{-}} \quad (1)$$

$$\tau_B = \frac{W_B^2}{2D_E} \quad (2)$$

A shallower pn-junction is more susceptible to thermally induced dopant diffusion and dopant counter-doping, which degrades device performance such as a lower breakdown voltage. Therefore, it is crucial to reduce the process temperature with more rigorous thermal budget control. However, reducing the deposition temperature introduces a new challenge of achieving silicon crystallization under such conditions. In the deposition of undoped silicon using a low-pressure chemical vapor deposition (LPCVD) technique, a temperature of approximately 600 °C or aggressive post-annealing is required to form polycrystalline silicon (p-Si), which is contradictory with the thermal budget constraints [1], [2]. If the growth temperature is below the critical point, silicon cannot easily nucleate and crystallize, which often leads to an amorphous film (a-Si) or a structural mixture of a-Si and p-Si, which has a higher film resistivity and slows down the device. Though by in-situ doping the critical temperature can be marginally lowered, which is via the introduction of additional nucleation sites and tensile stress in the film, the range of temperature is relatively limited [3], [4], [5], [6]. Moreover, excess dopant concentrations would suppress the nucleation process [7], [8].

There have been numerous studies that have focused on the active region of Heterojunction Bipolar Transistors (HBT), where silicon is grown epitaxially in an H_2 environment on single-crystal silicon (c-Si) [2], [6], [9], [10], [11], [12], [13], [14], [15], [16], [17]. However, there are very few studies that address silicon formation on dielectric materials such as silicon oxide and silicon nitride, which typically make up the extrinsic base area. Despite the film being doped heavily, the polycrystalline silicon regions are separated by amorphous film where dopant elements are not activated. As a result, the overall film resistance is high and affects the device performance [7].

The temperature during semiconductor growth plays a crucial role in determining the crystallization of silicon. When the temperature exceeds 600 °C, silicon atoms gain enough energy to surmount the activation energy barrier for crystallization, which allows them to move on the wafer surface and form a well-ordered, crystalline lattice structure. If a silicon film is deposited on c-Si under optimal conditions, the atoms can align with the underlying lattice structure, leading to the formation of a single-crystal layer, or epitaxial growth. Conversely, if the silicon film is deposited on dielectric materials, which possess random lattice structures, the silicon atoms tend to form short-range crystalline structures to minimize the overall energy of the system. However, as the process temperature is lowered, which results in a reduction in the kinetic energy of the silicon atoms, hindering their ability to move and form ordered structures. Hence, crystalline formation becomes increasingly challenging. At temperatures below a certain critical threshold, the silicon may not crystallize as there is insufficient thermal energy to overcome the barrier. In such cases, silicon remains in an amorphous state, which is characterized by a random arrangement of atoms, differing considerably from the regular lattice structure seen in crystalline silicon. Amorphous silicon exhibits distinct electrical properties, such as increased resistivity [53], [54].

There are proposed remedies to form a polycrystalline

This work was supported by the EDB-IPP under Grant No. REQ0377349. (Corresponding author: Wen Siang Lew)

Jingyan Huang is with GlobalFoundries Singapore (jingyan.huang@globalfoundries.com).

Kangjian Cheng and Wen Siang Lew are with the School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore (e-mail: kangjian001@e.ntu.edu.sg; wensiang@ntu.edu.sg).

silicon layer at reduced temperatures; however, these methods are not suitable for the specific requirements of forming the emitter and external base layers on a 40nm CMOS-HBT platform. One such method, Metal-Induced Crystallization (MIC), has the potential to lower the processing temperature to approximately 400°C to 600°C [18], [19], [20], [21], [22]. Despite this advantage, MIC introduces the risk of metal contamination during the front-end process, which can result in device leakage current and reliability concern [23], [24], [25]. Another alternative, Plasma Enhanced Chemical Vapor Deposition (PECVD), offers significant temperature reductions compared to Low Pressure Chemical Vapor Deposition (LPCVD) [26], [27], [28]. Nonetheless, PECVD would induce plasma damage to the underneath layer extending up to ~50nm, which could severely damage the thin base film in NPN devices, thereby compromising overall device performance [26], [29], [30], [31], [32].

Another category of approach involves forming of amorphous silicon at reduced process temperature, followed by recrystallization. This technique is commonly employed in the solar cell and Thin Film Transistor (TFT) industries through Excimer Laser Annealing (ELA) [33], [34], [35], [36], [37]. Nonetheless, the thickness of the recrystallization layer is directly proportional to the laser power [38], [39], [40]. In complex device structures, where amorphous silicon is present on both flat surfaces and sidewall regions, there is a risk of under-anneal or over-anneal (Fig. 1).

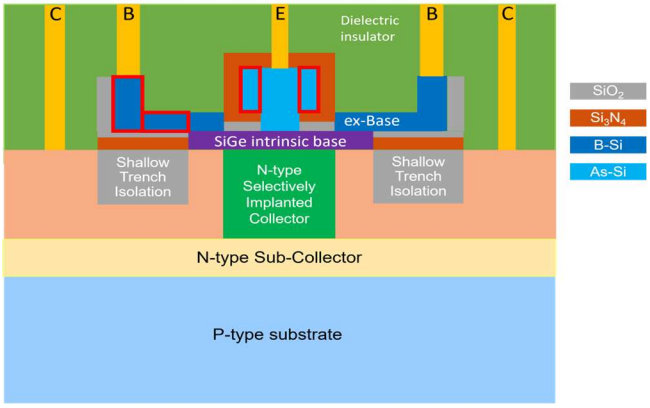

Fig. 1. Schematic illustration of a Collector-Base-Emitter-Base-Collector (CBEBC) Heterojunction Bipolar Transistor (HBT) NPN device. The area highlighted in red are the region of interest for this study.

Furthermore, it has been reported that the recrystallization through ELA can result in a segregation coefficient of less than unity and dopant pile up issue, which adversely affects the doping profile of the base layer [41], [42]. Hydrogen and other plasma surface treatments for recrystallization face similar challenges of plasma-induced defects [43], [44], [45], [46]. Also, the film after treatment is not fully crystallized and subsequent long annealing process is required [43], [44].

Lastly, Solid Phase Crystallization (SPC) is an established method for converting amorphous silicon into a crystalline state [47], [48], [49]. However, SPC necessitates long processing times of 10-72 hours at elevated temperatures more than 600°C [50], [51], [52]. This substantial thermal budget leads to undesirable dopant diffusion within the device, such as arsenic migration from the emitter into the base layer, and counter dope with boron.

Here, we demonstrate novel approaches for achieving uniform polycrystalline silicon for both n-type silicon with arsenic doping and p-type silicon with boron doping, while keeping the thermal budget to a minimum. The processed film exhibits a uniform structure with significantly reduced resistivity, which addresses the key challenges in current HBT fabrication processes, particularly those in the extrinsic base area. This development paves the way for technological advancements of HBT.

II. Experimental Setup and Methods

A 50 nm arsenic-doped silicon (As-doped Si) was deposited using an LPCVD technique, in which Si_2H_6 gas was used as the silicon precursor, and AsH_3 was introduced as an in-situ n-type dopant with a final arsenic doping concentration of 1×10^{20} atoms/cm^3. The deposition time was 100 seconds at a process pressure of ~100 Torr. For the boron-doped silicon (B-doped Si), a silicon thin film of 50~100 nm thickness was synthesized using the similar LPCVD technique. The silicon precursor employed was SiH_4, and BCl_3 was introduced as a p-type dopant with a final boron doping concentration of $\sim1\times10^{20}$ atoms/cm^3. The process was conducted at a constant pressure of ~1 Torr. A comprehensive structural characterization of the silicon films was conducted by using scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Standard four-point probe and ellipsometry techniques were used to measure the sheet resistance, thickness, and resistivity of the films.

Silicon deposited at low temperature (about 500 °C) has a bi-phase layer consisting of isolated polycrystalline particles dispersed on the smooth flat amorphous silicon matrix. The polycrystalline particles appear whitish, while the amorphous silicon matrix appears greyish. To quantify the proportion of polysilicon, the image underwent analysis using ImageJ software (Fig. 2). By setting an appropriate brightness threshold, polysilicon particles were selectively highlighted in red. The highlighted regions were then selected using the software's particle analysis function to obtain the area percentage of ~41.6%. This provides a valuable method for quantifying polysilicon content and evaluating the effectiveness of different processing conditions.

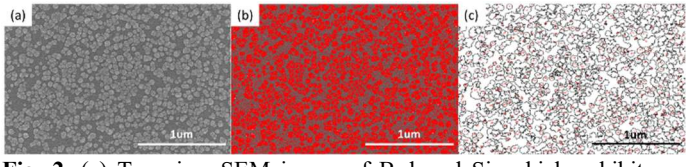

Fig. 2. (a) Top-view SEM image of B-doped Si, which exhibits a mixture of polycrystalline islands embedded in an amorphous film; (b) set suitable threshold value of brightness in ImageJ and highlight polycrystalline regions in red color; (c) ImageJ could select and calculate the area percentage of the highlighted region.

III. Impact of Process Temperature

The effects of temperature on the crystallization of silicon are shown in the TEM images of Fig. 3. The first row are cross-sectional TEM images of arsenic-doped silicon deposited on a silicon oxide layer at process temperatures of 500 °C, 550 °C, and 600 °C, respectively. At lower temperatures, the As-doped Si layer is amorphous with a uniform and smooth surface. As the temperature increases, crystallization begins at random nucleation sites, as seen in Fig. 3(b). This process leads to the emergence of polycrystalline regions that protrude noticeably, thereby changing the surface roughness. This increase in roughness is confirmed by atomic force microscopy (AFM) measurements in Fig. 4. Once crystallization completes, as depicted in Fig. 3(c), the roughness levels reduce again due to the uniformity in the height of the polycrystalline regions. Additionally, as shown in Fig. 5, the As-doped Si samples were subjected to X-ray diffraction (XRD) analysis to further support these observations. At lower deposition temperatures, the XRD spectra do not display any distinct peaks, indicating the amorphous nature of the material. However, as the process temperature increases, characteristic silicon peaks, such as (111) and (220) diffraction planes, begin to emerge, confirming the transition to a crystalline structure.

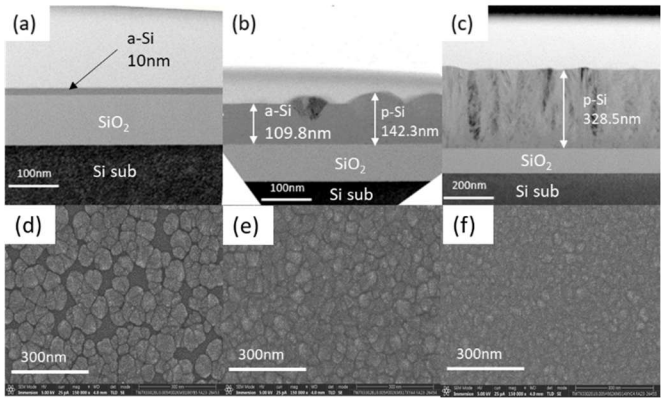

Fig. 3. Cross-section TEM images of As-doped Si deposited on 100nm silicon oxide at (a) 500 °C, (b) 550 °C and (c) 600 °C. The film deposited at different temperatures exhibits (a) amorphous, (b) mixture of a-Si and p-Si, and (c) fully polycrystalline structure, respectively. Top view of SEM of boron-doped Si deposited on silicon oxide at (d) 500 °C (e) 550 °C, and (f) 600 °C. The images reveal that the area of poly-Si increases with higher deposition temperature and eventually it saturates the whole film.

Similar analyses were performed on the boron-doped silicon (B- doped Si). Fig. 3 (d)-(e) displays top-view SEM images of B-doped Si deposited at 500 °C, 550 °C, and 600 °C. Remarkably, the boron-doped Si exhibits a higher degree of crystallization than the As-doped Si at the same temperatures. This may be due to the higher diffusion coefficient and lower epitaxial growth activation energy of boron, which can create nucleation sites more easily [48]. The SEM images also reveal the gradual evolution of the film, eventually becoming entirely occupied with polycrystalline regions.

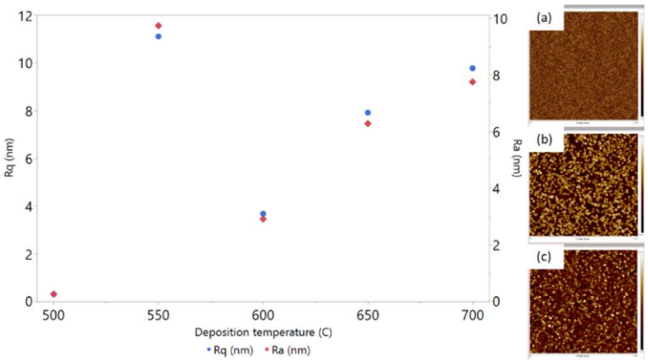

Fig. 4. Surface roughness Ra (average roughness) and Rq (root mean square roughness) at different deposition temperatures for As-doped Si. (a) At 500 °C, the surface is smooth with low roughness due to the amorphous nature of the film. (b) At 550 °C, the appearance of polycrystalline structures causes the highest roughness ~11nm observed. (c) At 600 °C, uniform crystallization leads to a smoother surface with reduced roughness, indicating a more homogeneous film thickness.

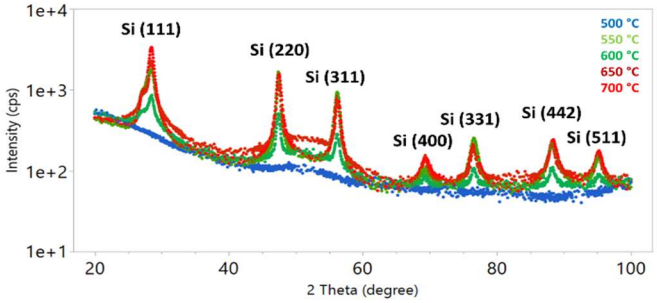

Fig. 5. XRD patterns of As-doped Si across varying deposition temperatures. At 500 °C, the absence of discernible peaks confirms the film's amorphous state. At 550 °C, the emergence of faint silicon peaks suggests the beginning of crystallization with a mix of amorphous and polycrystalline structures. At 600 °C, pronounced peaks indicate a transition to a predominantly crystalline silicon film.

The resistivity of the B-doped silicon films is significantly affected by their temperature-dependent morphology as shown in Fig. 6. At 500 °C, the presence of isolated polycrystalline silicon islands within an amorphous silicon matrix resulted in a resistivity of 127 mΩ·cm. However, when these polycrystalline regions become continuous, there is a significant decrease in resistivity to 9.31 mΩ·cm, indicating a substantial improvement by a factor of approximately 13.5. It is important to note that increasing the deposition temperature beyond the optimal point has an adverse effect on boron solubility, electrically active dopant and final charge carrier concentration, which leads to an increase in resistivity (Fig. 7) [55]. Therefore, for the in-situ boron-doped silicon, the optimum deposition temperature is limited to 550 °C. Similar temperature limitation is also observed for the arsenic-doped Si.

At 500 °C, the film predominantly exhibits an amorphous state, with boron dopants remaining inactive. The presence of isolated polycrystalline islands at this temperature leads to a high resistivity value of 127 mΩ·cm. At 550 °C, a significant change occurs as these polycrystalline regions begin to

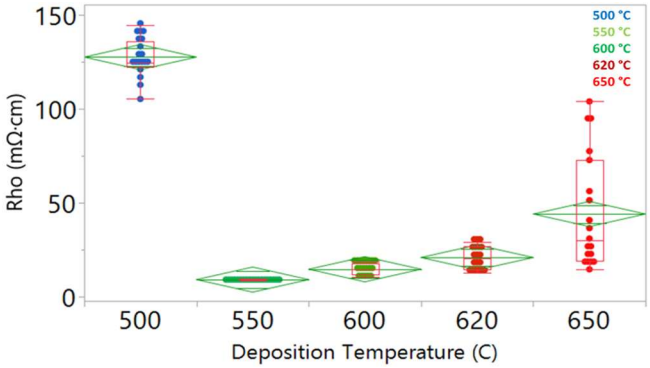

Fig. 6. Variation in film resistivity with deposition temperature in B-doped Si. Film resistivity increased from 9.31 mΩ·cm to 127 mΩ·cm when deposition temperature reduced from 550 °C to 500 °C.

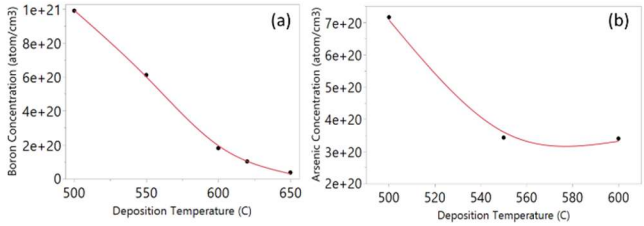

Fig. 7. Dopant concentration at different deposition temperatures for (a) B-Doped Si film and (b) As-Doped Si film. With higher temperatures, the dopant concentration decreases from 1E21 to 1E20 for and from 7E20 to 3E20 atom/cm^3, respectively.

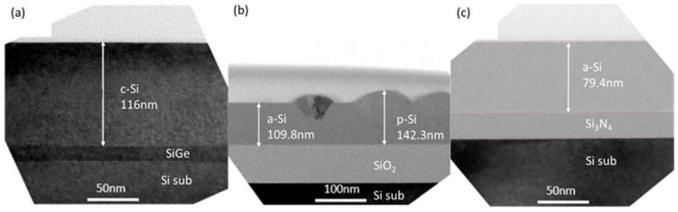

Fig. 8. Cross-sectional TEM images of the As-doped Si on different buffer layers. (a) 116nm Epitaxial growth is observed on HF-cleaned single crystal Si-SiGe substrate; (b) 142.3nm Polycrystalline film is observed on SiO_2 buffer layer; (c) 79.4nm Amorphous film is observed on Si_3N_4 buffer layer.

interconnect, enhancing the film's conductivity and reducing resistivity to 9.31 mΩ·cm. Beyond 550 °C, a decrease in boron dopant concentration is observed, which inversely affects the film's resistivity, causing it to increase once again.

IV. Impact of Buffer Layer on As-Doped Silicon

In the silicon deposition process used in HBT devices, the active device regions are exposed to single crystalline silicon. Concurrently, dielectric materials such as silicon oxide and silicon nitride are typically used as hard masks or spacer layers, and the choice of dielectric buffer layer can impact the crystallinity of the subsequently deposited silicon. This phenomenon is observed through TEM when As-Si is deposited on different substrates such as silicon, silicon oxide, and silicon nitride. Fig. 8 shows the impact of the buffer layer of silicon deposition under identical process conditions. A thin SiGe layer is firstly grown to distinguish between the substrate Si and subsequently epitaxy silicon cap. With a silicon buffer layer treated with hydrofluoric acid (HF), the wafer surface is free of foreign material and an epitaxial-like growth is observed, resulting in the formation of a single-crystal silicon layer, as shown in Fig. 8(a). However, when an amorphous silicon oxide buffer layer is used, the deposited As-Si initially exhibits an amorphous status as it has no existing crystalline order. When film thickness reaches ~50 nm, the nucleation and crystallization start at a random location, as shown in Fig. 8(b). In contrast, on the silicon nitride, the As-Si remains amorphous even when it reaches 80 nm. This could be due to silicon nitride having lower surface energy and considerable film stress, leading to a pronounced suppression of nucleation, culminating in the formation of an amorphous film. Silicon oxide, which shares more similar thermal expansion coefficients and other properties with silicon, moderately inhibits nucleation, albeit not completely precluding it. This partial suppression results in the emergence of island-like polycrystalline structures interspersed within an amorphous silicon matrix.

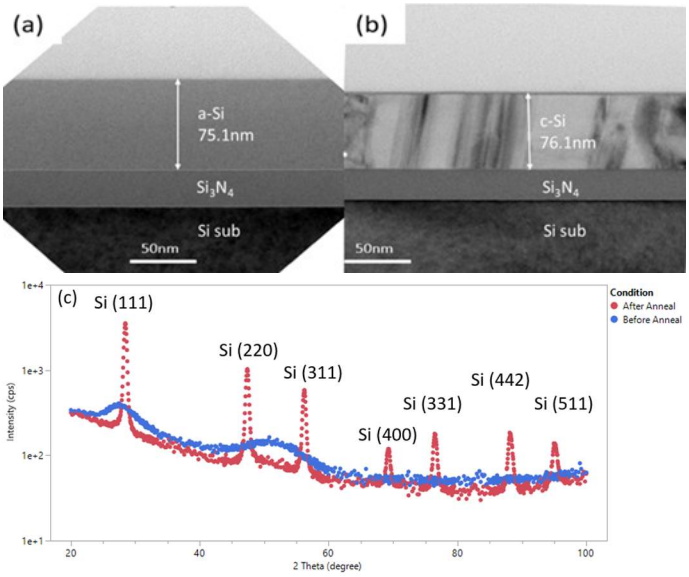

Fig. 9. Cross-sectional TEM image of the As-doped Si on silicon nitride, (a) before annealing and, (b) after annealing. (c) XRD analysis of the As-doped Si on silicon nitride before and after annealing.

Post-annealing is a common method used for recrystallizing amorphous films. Rapid thermal annealing such as 5s at 1000 °C can lead to a complete transformation of the As-doped Si film into a uniform polycrystalline layer, as confirmed by both TEM and XRD measurements in Fig. 9. This process results in a film resistivity of 1.10 mΩ·cm on nitride layer, which is about half of the resistivity obtained with a similar process on the oxide layer (1.84 mΩ·cm).

However, the ex-situ thermal annealing method applied to B-doped Si on the SiO_2 dielectric layer shows very little change in term of recrystallization after thermal annealing.

This may be due to the lack of the high free energy delta between fully amorphous Si and polycrystalline Si films. In addition, it requires a high thermal energy to break the existing short-range ordered crystalline islands [20], [21]. Based on these findings, it is suggested that using silicon nitride as dielectric hard mask layer leads to a uniform and low resistance subsequent As-doped Si film on dielectric materials. After subsequent deposition, the film remains uniform amorphous status. At downstream fabrication, a standard CMOS source/drain activation annealing process will automatically and effectively transform the arsenic-doped silicon into a continuous polycrystalline layer, characterized by enhanced uniformity and resistivity. Thus, no extra annealing process is required, and the overall thermal budget remains low.

V. Impact of Film Thickness on B-Doped Silicon

To achieve a uniform amorphous layer of B-doped Si, different alternatives can be considered, such as reducing the dopant concentration or lowering the processing temperature. Nonetheless, these approaches have their limitations: reducing the dopant concentration invariably increases the film's resistivity due to a reduction in acceptor dopants, and lowering the processing temperature can negatively impact productivity. Consequently, it is more beneficial to pursue methods that can directly form a uniform polycrystalline B-doped Si layer on dielectric materials without significantly increasing the thermal budget.

Our result reveals that nucleation commences midway through the film, which is consistent with reported findings [6], [56]. During the initial stages of film deposition, the thin silicon layer on silicon oxide induces high levels of film stress, which suppresses nucleation and leads to the formation of an amorphous layer. However, as the film thickness increases, newly deposited silicon atoms encounter an underlying layer of amorphous silicon instead of the dielectric material, mitigating the influence of buffer layer and initiating nucleation. Higher thickness and void development also help relieve in-film stress [14], [57], [58]. Additionally, cross-sectional TEM analysis reveals that the polycrystalline silicon adopts a cone-shaped morphology because of growth following nucleation. This structure results in a larger polycrystalline portion near the film's surface, which eventually covers the entire surface area. As the film thickness increases, not only does it promote the formation of new polycrystalline layers, but it also facilitates the crystal coalescence process of existing layers throughout the film.

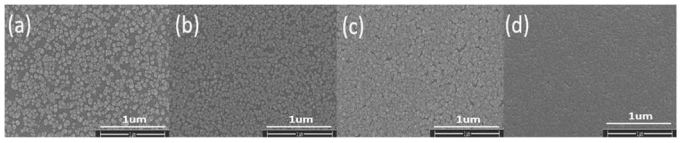

Fig. 10. Top view TEM image of B-doped Si on silicon oxide with different thicknesses. B-doped Si thickness increases from 500 Å to 1000 Å from (a) to (d), and the polycrystalline area percentage increases from ~40% to 100%.

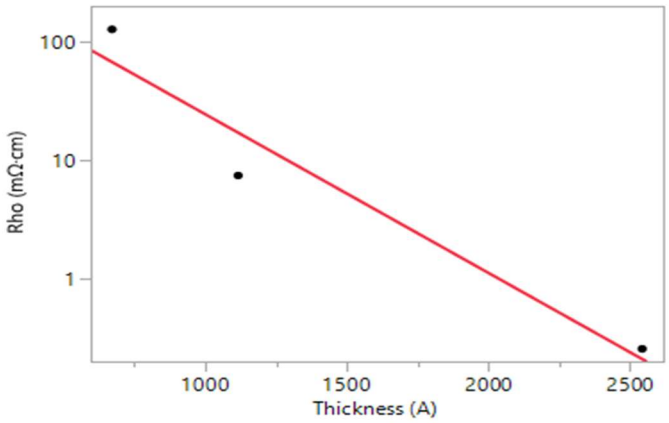

Fig. 11. Film resistivity of B-doped Si is inversely proportional to film thickness. At 2500 Å thickness, the resistivity is only 0.2% of the 650 Å film, using the same process temperature and gas flow setting.

Fig. 10 and Fig. 11 show a critical relationship between the film thickness and the extent of polycrystalline regions in silicon films. As the film thickness increases from 650 Å to 2500 Å, the measured resistivity decreases from 127 mΩ·cm to 0.254 mΩ·cm. This is a significant observation because the films were deposited at a reduced temperature of 500 °C, which means that they require less thermal energy to achieve low resistivity. This is an exciting enhancement from the previous lowest recorded resistivity value of 7.42 mΩ·cm at 550 °C. In addition, when compared to a film of 1100 Å thickness deposited at 500 °C, which is a twofold increase in thickness relative to our previous 670 Å standard, a 17-fold improvement in resistivity is observed. Furthermore, the influence of the extrinsic base area film thickness on device performance is secondary to that of film width. Thicker films facilitate a broader horizontal conduit for charge carriers, which enhances transport from the intrinsic base to the contact region. Nonetheless, this underscores the importance of a balanced approach in overall device structure design.

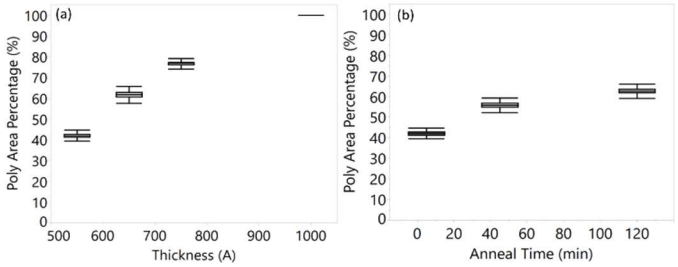

Fig. 12. (a) Percentage of polycrystalline area at different B-doped Si thickness, with 5 min in-situ annealing in nitrogen environment; (b) polycrystalline percentage for a 500 Å B-doped Si, with different annealing time in nitrogen environment.

To verify whether this higher percentage is due to the thermal budget or the film thickness, an in-situ N_2 annealing is conducted on B-doped Si with the same thickness. Fig. 12(b) shows that for boron-doped Si films with a thickness of 500 Å, the polycrystalline percentage reached a saturation point at ~65% after annealing for 120 mins, while increasing the film thickness to 1000 Å only required an additional 10 mins of

deposition time, as shown in Fig. 12(a). Hence, it is concluded that the higher polycrystalline percentage is primarily due to larger film thickness. In summary, augmenting the thickness of the boron film emerges as a straightforward and effective technique for fabricating a uniform polycrystalline B-doped Si layer, with minimal adverse effects.

VI. Conclusion

In conclusion, we have demonstrated a novel method for reduced-temperature growth of polycrystalline silicon films on dielectric materials, specifically for the development of advanced HBT devices. Uniform polycrystalline films are obtained for both n-type As-doped Si and p-type B-doped Si by optimizing the dielectric buffer layer and film thickness, adhering to a minimal thermal budget. This demonstrated growth technique has the potential to enhance the performance of HBT devices and contribute to the advancement of semiconductor device technology.

References

[1] T. Aoyama, G. Kawachi, N. Konishi, T. Suzuki, Y. Okajima, and K. Miyata, "Crystallization of LPCVD silicon films by low temperature annealing," *J. Electrochem. Soc.,* vol. 136, no. 4, pp. 1169-1173, 1989, doi: 10.1149/1.2096829.

[2] G. Harbeke, L. Krausbauer, E. F. Steigmeier, A. E. Widmer, H. F. Kappert, and G. Neugebauer, "Growth and physical properties of LPCVD polycrystalline silicon films," *J. Electrochem. Soc.,* vol. 131, no. 3, pp. 675-682, 1984, doi: 10.1149/1.2115672.

[3] C. Spinella, S. Lombardo, and F. Priolo, "Crystal grain nucleation in amorphous silicon," *J. Appl. Phys.,* vol. 84, no. 10, pp. 5383-5414, 1998, doi: 10.1063/1.368873.

[4] S. H. Sedani, O. F. Yasar, M. Karaman, and R. Turan, "Effects of boron doping on solid phase crystallization of in situ doped amorphous silicon thin films prepared by electron beam evaporation," *Thin Solid Films,* vol. 694, 2020, doi: 10.1016/j.tsf.2019.137639.

[5] T. Kobayashi, M. Koguchi, S. Iijima, M. Ohkura, and Y. Wada, "Nucleation of in-situ phosphorus-doped amorphous-silicon films depostied by pyrolysis of Si_2H_6 and PH_3," *J. Electrochem. Soc.,* vol. 141, no. 5, pp. 1365-1369, 1994, doi: 10.1149/1.2054925.

[6] S. Juneja and S. Kumar, "Boron induced crystallizaiton of silicon and glass: an alternative way to crystallize amorphous silicon films for solar cells," *Silicon,* vol. 9, no. 16, pp. 10459-10466, 2022, doi: 10.1007/s12633-022-01738-z.

[7] N. H. Pham *et al.*, "High thermoelectric power factor of p-type amorphous silicon thin films dispersed with ultrafine silicon nanocrystals," *J. Appl. Phys.,* vol. 127, no. 24, 2020, doi: 10.1063/5.0004318.

[8] S. Juneja, S. Sudhakar, J. Gope, K. Lodhi, M. Sharma, and S. Kumar, "Highly conductive boron doped micro/nanocrystalline silicon thin films deposited by VHF-PECVD for solar cell applications," *J. Alloys Compd,* vol. 643, pp. 94-99, 2015, doi: 10.1016/j.jallcom.2015.04.077.

[9] A. Pruijmboom *et al.*, "Heterojunction bipolar transistors with SiGe base grown by molecular beam epitaxy," *IEEE Electron Device Lett.,* vol. 12, no. 7, pp. 357-359, 1991, doi: 10.1109/55.103606.

[10] G. L. Patton, S. S. Iyer, S. L. Delage, S. Tiwari, and J. M. C. Stork, "Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy," *IEEE Electron Device Lett.,* vol. 9, no. 4, pp. 165-167, 1988, doi: 10.1109/55.677.

[11] R. Bhat, J. R. Hayes, E. Colas, and R. Esagui, "Atomic layer epitaxy grown heterojunction bipolar transistor having a carbon-doped base," *IEEE Electron Device Lett.,* vol. 9, no. 9, pp. 442-443, 1988, doi: 10.1109/55.6939.

[12] T. Sugii, T. Ito, Y. Furumura, M. Doki, F. Mieno, and M. Maeda, "Si heterojunction bipolar transistors with single-crystalline β-sic emitters," *J. Electrochem. Soc,* vol. 134, no. 10, pp. 2545-2549, 1987, doi: 10.1149/1.2100240.

[13] R. W. Collins *et al.*, "Evolution of microstructure and phase in amorphous, protocrystalline, and microcrystalline silicon studied by real time spectroscopic ellipsometry," *Sol. Energy Mater. Sol. Cells,* vol. 78, no. 1, pp. 143-180, 2003, doi: 10.1016/S0927-0248(02)00436-1.

[14] R. W. Collins *et al.*, "Real time analysis of amorphous and microcrystalline silicon film growth by multichannel ellipsometry," *Thin Solid Films,* vol. 364, no. 1, pp. 129-137, 2000, doi: 10.1016/S0040-6090(99)00925-6.

[15] S. Sriraman, S. Agarwal, E. S. Aydil, and D. Maroudas, "Mechanism of hydrogen-induced crystallization of amorphous silicon," *Nature,* vol. 418, no. 6893, pp. 62-65, 2002, doi: 10.1038/nature00866.

[16] H. Xu *et al.*, "Blue laser diode annealed top-gate low temperature poly-Si TFTs with low resistance of source/drain from deposited n+ layer," *IEEE J. Electron Devices Soc.,* pp. 1-1, 2024, doi: 10.1109/JEDS.2024.3392183.

[17] Y. -W. Liu *et al.*, "Single-crystal islands (SCI) for monolithic 3-D and back-end-of-line FinFET circuits," *IEEE Trans. Electron Dev.,* vol. 68, no. 10, pp. 5257-5262, 2021, doi: 10.1109/TED.2021.3101180.

[18] G. Ottaviani, D. Sigurd, V. Marrello, J. W. Mayer, and J. O. McCaldin, "Crystallization of Ge and Si in metal films. I," *J. Appl. Phys,* vol. 45, no. 4, pp. 1730-1739, 1974, doi: 10.1063/1.1663483.

[19] S.-W. Lee and S.-K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.,* vol. 17, no. 4, pp. 160-162, 1996, doi: 10.1109/55.485160.

[20] O. Nast, S. Brehme, D. H. Neuhaus, and S. R. Wenham, "Polycrystalline silicon thin films on glass by aluminum-induced crystallization," *IEEE Trans. Electron Dev.,* vol. 46, no. 10, pp. 2062-2068, 1999, doi: 10.1109/16.791997.

[21] J. Zhonghe, K. Moulding, H. S. Kwok, and M. Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films," *IEEE Trans. Electron Dev.,* vol. 46, no. 1, pp. 78-82, 1999, doi: 10.1109/16.737444.

[22] M. S. Abo Ghazala, H. A. Othman, L. M. Sharaf El-Deen, M. A. Nawwar, and A. El-hady B. Kashyout, "Fabrication of nanocrystalline silicon thin films utilized for optoelectronic devices prepared by thermal vacuum evaporation," *ACS Omega,* vol. 5, no. 42, pp. 27633-27644, 2020, doi: 10.1021/acsomega.0c04206.

[23] K. Graff, *Metal Impurities in Silicon-Device Fabrication (Springer Series in Materials Science, 24)*, 2nd, rev. ed.. Berlin: Springer, 2000.

[24] W. B. Henley, L. Jastrzebski, and N. F. Haddad, "Monitoring iron contamination in silicon by surface photovoltage and correlation to gate oxide integrity," *MRS Online Proceedings Library*, vol. 315, 299–312 (1993), https://doi.org/10.1557/PROC-315-299.

[25] D. Codegoni *et al.*, "Molybdenum contamination in silicon: detection and impact on device performances," *Solid State Phenom,* vol. 145-146, pp. 123-126, 2009, doi: 10.4028/www.scientific.net/SSP.145-146.123.

[26] M. Kondo, M. Fukawa, L. Guo, and A. Matsuda, "High rate growth of microcrystalline silicon at low temperatures," *J. Non-Cryst. Solids,* vol. 266, pp. 84-89, 2000, doi: 10.1016/S0022-3093(99)00744-9.

[27] K. Goshima *et al.*, "Lower temperature deposition of polycrystalline silicon films from a modified inductively coupled silane plasma," *Jpn. J. Appl. Phys.,* vol. 38, no. 6R A, pp. 3655-3659, 1999, doi: 10.1143/jjap.38.3655.

[28] P. R. Cabarrocas, A. Fontcuberta i Morral, B. Kalache, and S. Kasouit, "Microcrystalline silicon thin films grown by PECVD growth mechanisms and grain size control," *Solid State Phenom,* vol. 93, pp. 257-268, 2003.

[29] H. Kojima *et al.*, "Evaluation of damage in crystalline silicon substrate induced by plasma enhanced chemical vapor deposition of amorphous silicon films," *ECS J. Solid State Sci. Technol,* vol. 12, no. 1, p. 15003, 2023, doi: 10.1149/2162-8777/acb4bb.

[30] A. Piccirillo, R. Marzano, A. L. Gobbi, and P. E. Bagnoli, "Photoluminescence investigation of III-V semiconductor surface damage induced by PECVD silicon nitride films," *Appl. Surf. Sci.,* vol. 52, no. 4, pp. 295-302, 1991, doi: 10.1016/0169-4332(91)90071-Q.

[31] S. Li *et al.*, "Plasma-induced damage and annealing repairing in ALD-Al_2O_3/PECVD-SiN_x stacks," *Mater. Sci. Semicond. Process,* vol. 100, pp. 214-219, 2019, https://doi.org/10.1016/j.mssp.2019.05.010

[32] K. P. Cheung, "Mechanism of charging damage during plasma-enhanced silicon nitride/oxide thin-film deposition," *IEEE Trans. Device Mater. Rel.,* vol. 6, no. 3, pp. 448-454, 2006, doi: 10.1109/TDMR.2006.883545.

[33] Min Cao, S. Talwar, K. J. Kramer, T. W. Sigmon and K. C. Saraswat, "A high-performance polysilicon thin-film transistor using XeCl excimer laser crystallization of pre-patterned amorphous Si films," *IEEE Trans.*

Electron Dev., vol. 43, no. 4, pp. 561-567, 1996, doi: 10.1109/16.485538.

[34] Y. Sugawara, Y. Uraoka, H. Yano, T. Hatayama, T. Fuyuki, and A. Mimura, "Crystallization of double-layered silicon thin films by solid green laser annealing for high-performance thin-film transistors," *IEEE Electron Device Lett.,* vol. 28, no. 5, pp. 395-397, 2007, doi: 10.1109/LED.2007.895397.

[35] J. Liu *et al.*, "Preparation of large grain size polysilicon using long-pulse green laser annealing for 3-D integration technology," *IEEE Trans. Electron Dev.,* vol. 71, no. 3, pp. 1957-1962, 2024, doi: 10.1109/TED.2024.3360017.

[36] M. Choi, S. Lee, S. Kang, S. Jang, A. B. Siddik, and J. Jang, "High temperature solid phase crystallization of a-Si on glass by short time blue laser exposure for display backplane," *IEEE Electron Device Lett.,* vol. 43, no. 11, pp. 1890-1893, 2022, doi: 10.1109/LED.2022.3208832.

[37] M.-C. Nguyen et al., "Low-temperature deep ultraviolet laser polycrystallization of amorphous silicon for monolithic 3-dimension integration," *IEEE Electron Device Lett.,* vol. 42, no. 6, pp. 784-787, 2021, doi: 10.1109/LED.2021.3074627.

[38] L. Jastrzebski, A. E. Bell, and C. P. Wu, "The depth of defect annihilation in silicon by pulse laser annealing: Experiment and theory," *Appl. Phys. Lett.,* vol. 35, no. 8, pp. 608-611, 1979, doi: 10.1063/1.91225.

[39] M. Toulemonde, R. Heddache, F. Nielsen, and P. Siffert, "Direct measurement of the maximum depth phase change of crystal silicon under pulsed laser irradiation," *J. Appl. Phys.,* vol. 56, no. 6, pp. 1878-1880, 1984, doi: 10.1063/1.334204.

[40] G. Fisicaro and A. La Magna, "Modeling of laser annealing," *J. Comput. Electron,* vol. 13, no. 1, pp. 70-94, 2014, doi: 10.1007/s10825-013-0545-9.

[41] K. K. Ong, K. L. Pey, P. S. Lee, A. T. S. Wee, X. C. Wang, and Y. F. Chong, "Dopant distribution in the recrystallization transient at the maximum melt depth induced by laser annealing," *Appl. Phys. Lett.,* vol. 89, no. 17, pp. 172111-172111-3, 2006, doi: 10.1063/1.2364834.

[42] J.-I. Chikawa and F. Sato, "Impurity incorporation at melt-crystal interfaces in pulsed laser annealing of silicon," *Jpn. J. Appl. Phys.,* vol. 19, no. 3, pp. L159-L162, 1980, doi: 10.1143/JJAP.19.L159.

[43] H. P. Zhou *et al.*, "Hydrogen-plasma-induced rapid, low-temperature crystallization of μm-thick a-Si:H films," *Sci. Rep,* vol. 6, no. 1, pp. 32716-32716, 2016, doi: 10.1038/srep32716.

[44] K. Pangal, J. C. Sturm, and S. Wagner, "Effect of plasma treatment on crystallization behavior of amorphous silicon films," *MRS Online Proceedings Library,* vol. 507, pp. 577-582, 1998, doi: 10.1557/PROC-507-577.

[45] K. Pangal, J. C. Sturm, S. Wagner, and T. H. Büyüklimanli, "Hydrogen plasma enhanced crystallization of hydrogenated amorphous silicon films," *J. Appl. Phys.,* vol. 85, no. 3, pp. 1900-1906, 1999, doi: 10.1063/1.369182.

[46] S. J. Jeng, G. S. Oehrlein, and G. J. Scilla, "Hydrogen plasma induced defects in silicon," *Appl. Phys. Lett.,* vol. 53, no. 18, pp. 1735-1737, 1988, doi: 10.1063/1.99810.

[47] D. L. Young *et al.*, "Rapid solid-phase crystallization of high-rate, hot-wire chemical-vapor-deposited hydrogenated amorphous silicon," *Appl. Phys. Lett.,* vol. 89, no. 16, 2006, doi: 10.1063/1.2361163.

[48] G. L. Olson and J. A. Roth, "Kinetics of solid phase crystallization in amorphous silicon," *Mater. Sci. Rep.,* vol. 3, no. 1, pp. 1-77, 1988, doi: 10.1016/S0920-2307(88)80005-7.

[49] L. Haji, P. Joubert, J. Stoemenos, and N. A. Economou, "Mode of growth and microstructure of polycrystalline silicon obtained by solid-phase crystallization of an amorphous silicon film," *J. Appl. Phys.,* vol. 75, no. 8, pp. 3944-3952, 1994, doi: 10.1063/1.356014.

[50] K. Sharma, A. Branca, A. Illiberi, F. D. Tichelaar, M. Creatore, and M. C. M. van de Sanden, "On the effect of the amorphous silicon microstructure on the grain size of solid phase crystallized polycrystalline silicon," *Adv. Energy Mater.,* vol. 1, no. 3, pp. 401-406, 2011, doi: 10.1002/aenm.201000074.

[51] S. Hasegawa, T. Nakamura, and Y. Kurata, "Axially controlled solid-phase crystallization of amorphous silicon," *Jpn. J. Appl. Phys.,* vol. 31, no. 2R, pp. 161-167, 1992, doi: 10.1143/JJAP.31.161.

[52] E. Korin, R. Reif, and B. Mikic, "Crystallization of amorphous silicon films using a multistep thermal annealing process," *Thin Solid Films,* vol. 167, no. 1, pp. 101-106, 1988, doi: 10.1016/0040-6090(88)90486-5.

[53] J. B. Boyce *et al.*, "Laser doping and crystallization of amorphous silicon thin films," *MRS Online Proceedings Library,* vol. 358, 1994, doi: 10.1557/PROC-358-909.

[54] R. Morimoto, A. Izumi, A. Masuda, and H. Matsumura, "Low-resistivity phosphorus-doped polycrystalline silicon thin films formed by catalytic chemical vapor deposition and successive rapid thermal annealing," *Jpn. J. Appl. Phys.,* vol. 41, no. 2 A, pp. 501-506, 2002, doi: 10.1143/jjap.41.501.

[55] B.-J. Jin, W.-E. Hong, D. H. Kim, T. Uemoto, C. W. Kim, and J.-S. Ro, "Reverse annealing of boron doped polycrystalline silicon," *Thin Solid Films,* vol. 516, no. 18, pp. 6321-6324, 2008/07/31/ 2008, doi: https://doi.org/10.1016/j.tsf.2007.12.120.

[56] G. v. Elzakker, F. D. Tichelaar, and M. Zeman, "Suppression of crystalline growth in silicon films deposited from hydrogen diluted silane using a layer-by-layer approach," *Thin Solid Films,* vol. 515, no. 19, pp. 7460-7464, 2007, doi: 10.1016/j.tsf.2006.11.114.

[57] J. Koh, Y. Lee, H. Fujiwara, C. R. Wronski, and R. W. Collins, "Optimization of hydrogenated amorphous silicon p-i-n solar cells with two-step i layers guided by real-time spectroscopic ellipsometry," *Appl. Phys. Lett.,* vol. 73, no. 11, pp. 1526-1528, 1998, doi: 10.1063/1.122194.

[58] J. Koh, A. S. Ferlauto, P. I. Rovira, C. R. Wronski, and R. W. Collins, "Evolutionary phase diagrams for plasma-enhanced chemical vapor deposition of silicon thin films from hydrogen-diluted silane," *Appl. Phys. Lett.,* vol. 75, no. 15, pp. 2286-2288, 1999, doi: 10.1063/1.124992.