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Nanoporous Cation Limiter-Induced Enhancement of Threshold Switching and Oscillatory Behavior in Ag-Based Diffusive Memristors

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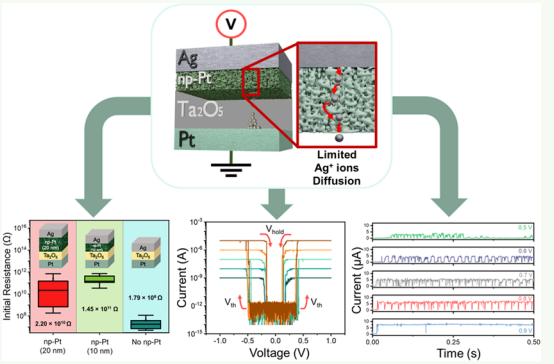
ABSTRACT: The development of memristors for neuromorphic computing has gained attention due to their ability to mimic biological neurons. Among the various switching mechanisms, volatile electrochemical metallization (ECM)-threshold switching (TS) memristors show promise for artificial neural networks due to their simple structure and low operating voltages. However, ECM TS memristors often suffer from poor switching uniformity, limiting practical applications. In this work, we demonstrate a highly uniform switching Ag-based TS memristor with a nanoporous-Pt (np-Pt) cation limiter. The device achieves ultralow leakage current (<1 pA), high selectivity (>10^7), and high endurance (>10^6 cycles). The np-Pt cation limiter also enhances the device's stability by reducing variability in the operating voltages (V_{th} and V_{hold}) and enabling operations at higher current compliance levels (∼10 μA). In addition, the Ag/np-Pt TS device exhibits self-oscillation behavior at low voltage (<1 V), with oscillation frequency increasing with the applied voltage. The insertion of the np-Pt cation limiter provides a simplistic technique of metal ions manipulation in ECM TS devices, enhancing their performance for artificial neural network applications.



KEYWORDS: *diffusive memristor, nanoporous platinum, threshold switching, neuronal, silver, ECM*

1. INTRODUCTION

In the era of big data, threshold switching (TS) memristors have emerged as essential components for memristive functionality, particularly in nonconventional computing and nonvolatile memory applications.[1−4] Nonconventional computing architectures, such as spiking neural networks (SNNs), mimic neural activity patterns in human cognition by leveraging asynchronous and sparse spikes.[5−7] From a hardware implementation perspective, it is imperative to explore artificial synapses and neurons for the advancement of neuromorphic systems. To date, the emulation of biosynaptic functions using artificial synapses has been predominantly achieved through resistive switching (RS) memristors, facilitating functionalities such as spike-time-dependent plasticity (STDP),[8,9] pair-pulse facilitation/depression (PPF/PPD),[10,11] and long-term potentiation/depression (LTP/LTD).[12,13] Conversely, artificial neurons typically rely on intricate complementary metal-oxide-semiconductor (CMOS) circuits comprising of numerous active components to implement neuronal functions. However, these configurations are often plagued by low energy efficiency and constrained integration density.[14−17]

Recently, TS memristors have garnered attention due to their large selectivity, simple structure, and scaling capability, positioning them as promising candidates in applications such as selectors for nonvolatile data storage,[18−20] steep slope transistors for logic devices,[21,22] and neurons for neuromorphic computing. Various materials have been explored for TS memristors, including insulator−metal-transition (e.g., NbO_2 and VO_2),[23−25] chalcogenide (e.g., GeSe),[26,27] and transition metal oxide (e.g., TaO_x and HfO_2),[28,29] with several studies demonstrating their potential for exhibiting oscillatory behavior, a key characteristic for neuromorphic applications. Ta_2O_5 is widely recognized as a highly promising solid electrolyte for TS memristors owing to its high ionic conductivity and robust stability. However, these devices often suffer from high operational voltage and large leakage current, leading to higher power consumption.[30]

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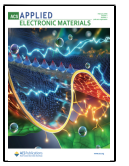

Volatile electrochemical metallization (ECM) TS memristors, which utilize Ag or Cu, offer the advantages of lower operation voltage, steep switching slope, and lower leakage current characteristics.[22,31,32] These attributes are preferential for the implementation of neuromorphic systems, as they offer fast recognition speed and low power consumption. Unlike conventional nonvolatile ECM memristors, which operate on the formation and dissolution of stable conductive filaments.[33,34] Volatile ECM TS devices have a conductive filament that undergoes spontaneous rupture, resulting in the threshold switching phenomenon. However, large variability in size and distribution of the stochastic conductive filaments still exists which greatly hinders large-scale integration in practical crossbar arrays.[33,35] Furthermore, it is observed that a volatile threshold switching often transitions to a nonvolatile resistive state upon continuous cycling, a phenomenon attributed to the stable growth of filaments within the dielectric matrix.[19,36] It is noteworthy that a highly stable metal filamentary TS with low threshold voltage and minimal off-state leakage current is much preferred as it correlates to a broader weight range for oscillatory neuronal functions.[37]

To address these challenges, recent studies have explored the use of interfacial layers, such as Ir, Ti, and graphene, to improve the uniformity and stability of TS devices.[38−40] Among these materials, Pt has shown promise due to its high work function (∼5.8 eV) which surpasses those of Ti (∼4.3 eV), Ir (∼5.4 eV), and graphene (∼4.6−4.8 eV), resulting in a larger Schottky barrier at the Ta_2O_5 interface. This effectively suppresses leakage currents and improves cation migration control, crucial for reliable threshold switching.[41] Additionally, Pt's lower Gibbs free energy of oxide formation (e.g., PtO_2, $\Delta G^0 \approx -121$ kJ/mol) compared to TiO_2 ($\Delta G^0 \approx -889.5$ kJ/mol) and IrO_2 ($\Delta G^0 \approx -183.75$ kJ/mol) minimizes oxide formation, preserving metallic properties under operating conditions.[42] Furthermore, np-Pt can be fabricated via scalable, reproducible methods like high-pressure sputtering, unlike graphene, which requires less practical approaches such as chemical vapor deposition (CVD).[43,44] However, there has not yet been a reported investigation on how the nanoporous-Pt (np-Pt) interfacial layer influences the memristive properties of ECM TS devices.

In this work, we present an oscillatory neuron based on Ag filamentary TS with a nanoporous-Pt (np-Pt) cation limiter that modulates the Ag cation migration. To increase the porosity of the Pt interfacial layer, the sputter pressure is increased from 2 to 20 mTorr.[45] Tuning the np-Pt thickness leads to the formation of a significantly more stable conductive filament. 10 nm np-Pt devices demonstrate large selectivity ($\sim 10^7$), ultralow leakage current (<1 pA), improved operational voltage uniformity, high endurance cycle (>10^6 cycles), and a minimized operating current of 1 nA. Moreover, the 10 nm np-Pt TS device exhibits self-oscillation behavior at a low voltage (<1 V), where the oscillation frequency increases with the applied voltage.

A simplified biological neuron network is illustrated in Figure 1a, where a neuron receives input spikes from interconnected synapses, triggering an output action potential upon reaching a threshold value. Contrastingly, Figure 1b depicts the equivalent TS neuronal network within an artificial neural network framework, where the RS memristors act as artificial synapses connecting pre-neurons and post-neurons. The TS memristor functions as a post-neuron, integrating the signals from these artificial synapses. The circuit implementation of the oscillation neuron based on the TS memristor is shown in Figure 1c. The load resistance R_L represents the RS memristor synaptic weight connected in series with the TS device while the load capacitance C_L represents the parallel capacitance and parasitic capacitance. In the absence of an applied electric field, the TS device remains in the OFF state (R_{OFF}). Upon the application of a voltage pulse (V_{in}), the voltage drops over the TS device ($R_{OFF} > R_L$) and C_L starts to charge. If V_{in} surpasses the threshold voltage (V_{th}), the TS device switches to the ON state (R_{ON}), causing C_L to discharge as the voltage drop across the TS device decreases ($R_{ON} < R_L$). When the voltage drop falls below the hold voltage (V_{hold}), the TS device switches back to R_{OFF}. In this recursive event where the TS device switches between the OFF and ON state, self-oscillation characteristics can be achieved. For $R_{OFF} \gg R_L \gg R_{ON}$, the relationship between the theoretical frequency f and the R_L, C_L, and V_{in} can be described as follows:[24]

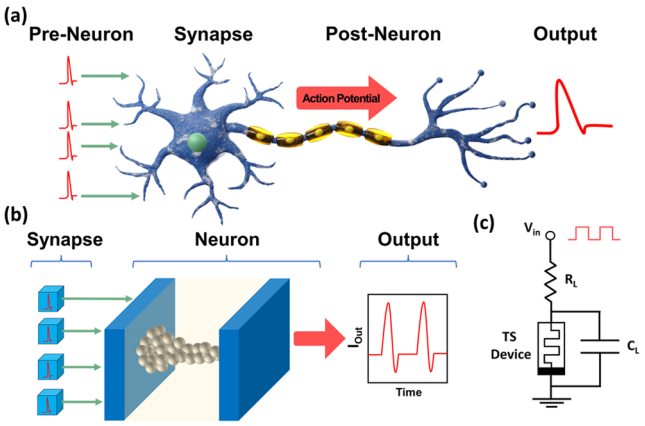

Figure 1. Schematic illustration of neuromorphic system. (a) Biological model: the biological neuron receives inputs from other neurons by interconnected synapses. (b) Bio-inspired electronic model: the electronic neuron for accumulating inputs generated by different pre-neurons through resistive switching (RS) memristor synapses to implement the functions of spiking neural network. (c) Circuit implementation of the oscillation neuron with a TS memristive device.

$$f = \frac{1}{\left[R_L C_L \times \log\left(\frac{V_{hold} - V_{in}}{V_{th} - V_{in}}\right)\right]} \quad (1)$$

2. EXPERIMENT PREPARATION

The fabrication process of the np-Pt TS devices on the SiO_2/Si substrate begins with a cleaning procedure using acetone, 2-propanol, and deionized water. Following this, Pt bottom electrode (10 nm) is deposited on the patterned SiO_2/Si substrates at room temperature by direct current (DC) magnetron sputtering, utilizing a 2 in. 99.99% target of Pt, at a power of 50 W, a sputtering pressure of 2 mTorr, and an Ar gas flow of 20 sccm. The patterned Pt bottom electrode is formed via a liftoff process. Next, the active electrode patterning is performed, followed by a Ta_2O_5 thin film (5 nm), np-Pt layer (10 and 20 nm), and Ag active electrode deposition. The Ta_2O_5 thin film is deposited via radio frequency (RF) magnetron sputtering with 20 sccm Ar gas flow at a working pressure of 2 mTorr, utilizing a 2 in. 99.99% ceramic target of Ta_2O_5. The np-Pt layers are deposited with similar sputtering conditions, except for an elevated sputter

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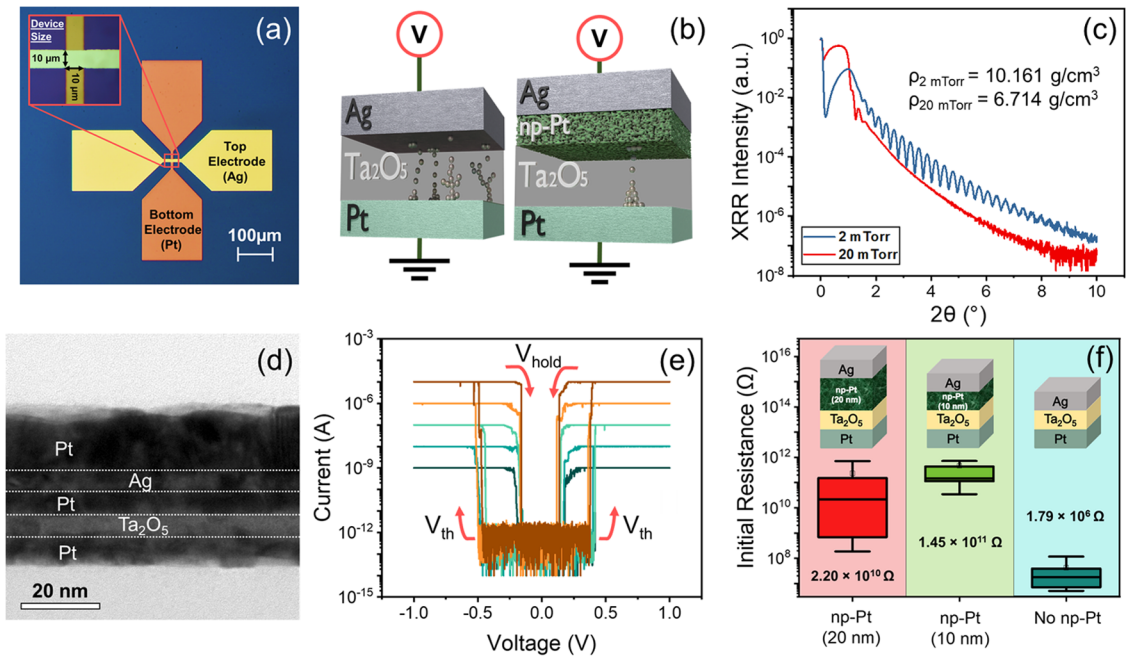

Figure 2. (a) Optical image of a fabricated np-Pt layer TS device. (b) Schematic illustration of the different resistive switching mechanisms in the no np-Pt (left) and np-Pt-based (right) devices. (c) XRR measurement of 10 nm of Pt sputtered at 2 mTorr (blue) and 20 mTorr (red). (d) Cross-sectional TEM image of the 10 nm np-Pt TS device. (e) Typical current−voltage (I−V) curves for 10 nm np-Pt layer TS device under different compliance current conditions from 1 nA to 10 μA. (f) Initial resistance of five TS devices with different thicknesses of np-Pt (20 nm, 10 nm, and no np-Pt).

pressure of 20 mTorr to induce porosity. The Ag (5 nm) layer is deposited by DC magnetron sputtering, followed by a Pt capping layer (20 nm) to protect the underlying Ag from ambience oxidation. A 2 in. 99.99% Ag target was utilized. A final liftoff process is performed to obtain the Pt/Ag/np-Pt/Ta_2O_5/Pt device with a size of 10 × 10 μm^2, as depicted in Figure 2a. For the deposition of all of the thin films, the AJA sputtering system was employed.

3. RESULTS AND DISCUSSION

Figure 2b illustrates the limited Ag cation injection by the np-Pt layer between the cation source and the electrolyte layer. For the characterization of the np-Pt's surface morphology, atomic force microscopy (AFM) scans were performed using the Park Systems NX 10 while the X-ray reflectivity (XRR) measurements were performed using Rigaku SmartLab. The AFM scans are presented in Figure S1. XRR characterization, as shown in Figure 2c, determined that the density of the Pt thin film sputtered at 20 mTorr ($\rho_{20\,mTorr}$ = 6.714 g/cm^3) is substantially lower than that of the film sputtered at 2 mTorr ($\rho_{2\,mTorr}$ = 10.161 g/cm^3), suggesting that the higher sputtering pressure produces a more porous Pt film. Cross-sectional transmission electron microscopy (TEM) was performed to understand the profile, as shown in Figure 2d, where the Ag layer is effectively isolated from the Ta_2O_5 layer by the np-Pt cation limiter. The dark-field TEM image is presented in Figure S2. In addition, energy-dispersive X-ray (EDX) line scan analysis was also performed and the results are presented in Figure S3. Figure 2e presents the typical current−voltage (I−V) electrical characteristics of the 10 nm np-Pt TS device under voltage sweeps between −1 and +1 V, with a resolution of 5 mV, and at different compliance current (I_C) values from 1 nA to 10 μA. The measurements are performed using the Keithley 4200-SCS semiconductor characterization system. When the applied voltage surpasses the threshold voltage (V_{th}), the device switches abruptly from HRS to LRS with the current level predetermined by I_C. Upon reducing the applied voltage below the hold voltage (V_{hold}), the device reverts back to the HRS. The 10 nm np-Pt TS device exhibits bidirectional switching characteristics, with a large selectivity of 10^7 at the maximum compliance current of 10 μA. For comparison, the typical I−V characteristics of devices without np-Pt and with a 20 nm np-Pt layer are shown in Figure S4.

Figure 2f shows the boxplot of the initial resistance values for the TS devices with different thicknesses of the np-Pt layer, measured at a read voltage is 0.1 V. Among the different thicknesses of np-Pt layer, the 10 nm np-Pt TS device exhibits the highest initial resistance of 1.45 × 10^{11} Ω, which is significantly higher than the initial resistance of 1.79 × 10^6 Ω for the device without an np-Pt layer. The increased initial resistance suggests that the diffusion of Ag into the dielectric matrix is limited by the np-Pt layer. For comparative purposes, a 20 nm np-Pt TS device was also fabricated, showing an initial resistance of 2.20 × 10^{10} Ω. However, this device exhibited a broader distribution of initial resistance and a lower initial resistance relative to the 10 nm np-Pt device. This performance degradation could be due to the increased surface roughness observed in the 20 nm np-Pt thin film (R_a = 1.277 nm, R_q = 1.020 nm) [Figure S1b], as compared to the smoother surface of the 10 nm np-Pt thin film (R_a = 0.446 nm, R_q = 0.572 nm) [Figure S1a]. Increased surface roughness generally reduces the memristive properties, as it can lead to less uniform electrical characteristics across the device.[46] However, in this case, the rougher surface of the np-Pt layer enhances the effective contact area with the Ag top electrode, promoting improved charge carrier injection which reduces the initial resistance.[47,48]

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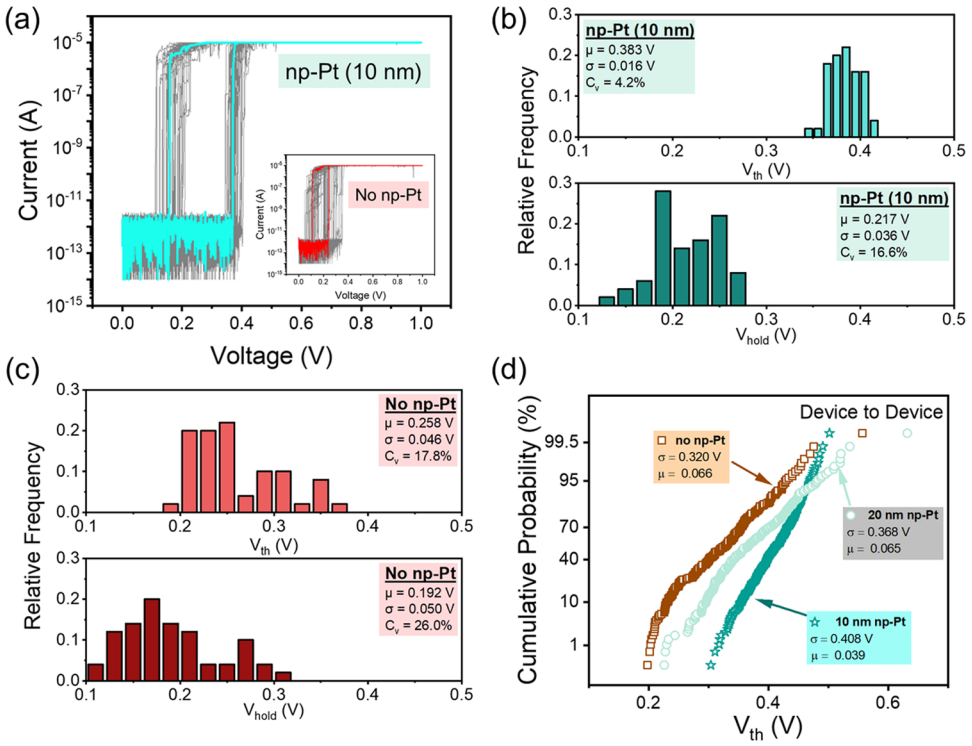

Figure 3. (a) Unidirectional DC $I-V$ characteristics of a 10 nm np-Pt TS device in 50 cycles of DC voltage sweep. Light blue represents the typical TS operation. The inset provides the unidirectional DC $I-V$ characteristics of no np-Pt TS device in 50 cycles of DC voltage sweep. (b) Statistical distributions of the operational voltages ($+V_{th}$, $+V_{hold}$) for a 10 nm np-Pt TS device (sample size n = 50). (c) Statistical distribution of the operational voltages ($+V_{th}$, $+V_{hold}$) for no np-Pt TS device (sample size n = 50). (d) Cumulative probability distribution of V_{th} (device-to-device) for different np-Pt thicknesses (sample size n = 5).

Unidirectional threshold switching is observed in the 10 nm np-Pt TS device, as shown in Figure 3a, where the device exhibits uniform threshold switching behavior over 50 consecutive cycles. To further evaluate the cycle-to-cycle variation of 10 nm np-Pt TS device, the distributions of V_{th} and V_{hold} in the positive voltage region over these 50 cycles are analyzed and presented in Figure 3b. The standard deviation (σ), mean value (μ), and coefficient of variation ($C_V = \sigma/\mu$) are used to evaluate the variations. The C_V values for V_{th} and V_{hold} are 4.2 and 16.6%, respectively. The distributions of V_{th} and V_{hold} in the negative voltage region are also plotted in Figure S5a.

Figure 3c shows the statistical distributions of V_{th} and V_{hold} for TS device without np-Pt layer in the same scale, where the C_V values are 17.8% and 26.0%, respectively. By comparison, the no-Pt TS device shows a much larger variation, with C_V for V_{th} and V_{hold} increasing by 423.9% and 156.6%, respectively. While a lower C_V of V_{hold} (10.7%) is observed for the 20 nm np-Pt TS device, this improvement comes with an increase in the C_V of V_{th} (9.0%). The statistical distributions of V_{th} and V_{hold} for 20 nm np-Pt TS device are also analyzed and shown in Figure S5b. A cumulative probability distribution for the cycle-to-cycle variation of the V_{th} for the different np-Pt thicknesses is shown in Figure S6a. The σ, μ, and C_V for the TS device with different np-Pt thicknesses are summarized in Table 1.

Figure 3d shows the device-to-device variation for both the no np-Pt and 10 nm np-Pt TS devices, where five random devices are selected from each type of TS memristors. The no np-Pt TS devices, despite having a lower mean V_{th} of ~0.32 V, show a much larger device-to-device variation (C_V = 20.6%). This variability can be attributed to uncontrolled Ag cation injection throughout the Ta_2O_5 matrix. As for the 10 nm np-Pt TS devices, a mean V_{th} of ~0.41 V is shown along with tight distributions (C_V = 9.6%), indicating limited Ag cation injection into the Ta_2O_5 matrix. A further increase of np-Pt thickness to 20 nm results in a reduced mean V_{th} of ~0.37 V. However, a degradation of the device performance is observed where the V_{th} shifts into a wider range from device to device (C_V = 17.7%). Conversely, the 10 nm np-Pt TS devices reveal the narrowest V_{th} distribution, as compared with the no np-Pt and 20 nm np-Pt TS devices, as shown in Figure S6b.

Table 1. Comparison of Mean, Standard Deviation, and Coefficient Of Variation for V_{th} and V_{hold} in the Positive Region (Cycle-to-Cycle Variation)

np-Pt thickness (nm)	V_{th}, μ (V)	V_{hold}, μ (V)	V_{th}, σ (V)	V_{hold}, σ (V)	V_{th}, $C_V = \sigma/\mu$	V_{hold}, $C_V = \sigma/\mu$
0	0.258	0.192	0.046	0.050	17.8%	26.0%
10	0.383	0.217	0.016	0.036	4.2%	16.6%
20	0.399	0.307	0.037	0.033	9.0%	10.7%

Figure 4a shows the DC stress test conducted on the 10 nm np-Pt device at room temperature, revealing that the HRS remains stable for over 10^4 s without any noticeable degradation under a bias voltage of 0.2 V. For endurance measurements, consecutive read and program-read pulses are applied across the device, as shown in Figure 4b. A read pulse of 0.3 V/1 ms is applied to determine the HRS with a 1 ms delay before a program-read pulse of 0.9 V/5 ms is applied to switch the device to the LRS. A series resistor of 220 kΩ is connected to limit the current in the LRS during the measurement. A waiting time of 100 ms separating each

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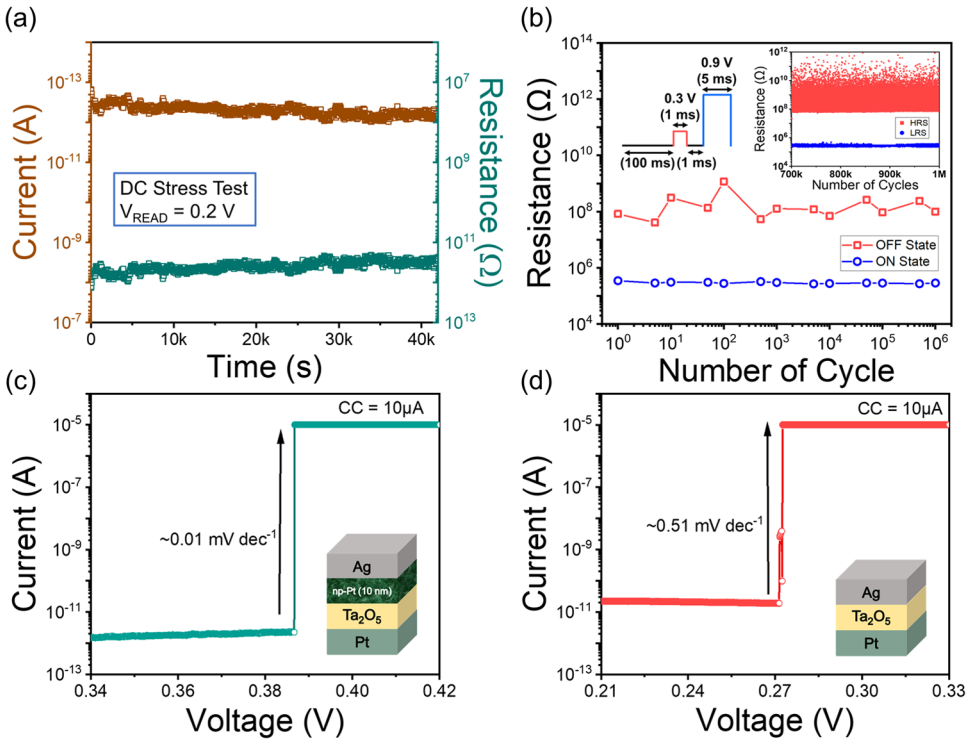

Figure 4. (a) DC stress testing at room temperature for a 10 nm np-Pt TS device. Green squares and brown squares refer to the current at HRS and resistance value of HRS, respectively. (b) Endurance test of the 10 nm np-Pt TS device with over 10^6 cycles, where the inset shows all of the HRS and LRS data points for the last 300,000 cycles. (c) ON switching slope of the 10 nm np-Pt TS device is approximately 0.01 mV/dec (d) ON switching slope of the no np-Pt TS device is approximately 0.51 mV/dec.

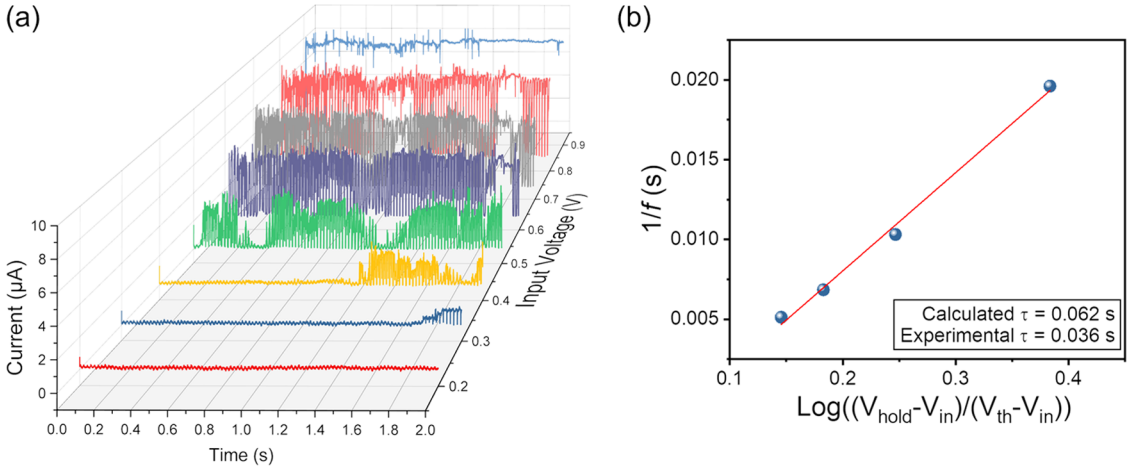

Figure 5. (a) Oscillation waveforms of the 10 nm np-Pt TS neuron with different V_{in}'s from 0.2 to 0.9 V when R_L = 180 kΩ, C_L = 200 nF. (b) Fitted oscillation frequency, f versus input voltage, and V_{in} plot corresponding to the measured oscillation frequencies.

program and read pulse ensures that the device recovers fully, avoiding the memory effect from unsuccessful switching events. The device demonstrates stable switching for more than 1×10^6 cycles without noticeable degradation. The inset shows every data point for HRS and LRS from the last 300,000 endurance cycles. The presented endurance data represent the lower bound, as the measurement was terminated due to schedule constraints. In addition, the 10 nm np-Pt device can switch abruptly at an I_C of 10 μA and exhibits a high selectivity of 1×10^7, as shown in Figure 4c. The device exhibits a steeper switching slope of ~0.01 mV/dec as compared with the no np-Pt device (~0.51 mV/dec), as shown in Figure 4d. The switching slopes of the 10 nm np-Pt TS device at other I_C values are shown in Figure S7. The acceleration in the switching slope can be attributed to the galvanic effect, where the electrochemical oxidation of Ag atoms takes precedence over Pt atoms due to their respective electrode potentials ($E_{0,Ag^{2+}/Ag}$ = 0.80 V and $E_{0,Pt^{2+}/Pt}$ = 1.18 V).[49,50]

Based on the TS characteristics of the 10 nm np-Pt TS device, an oscillation neuron was further constructed, as shown in Figure 1c. The np-Pt TS device was connected in parallel with a load capacitance (C_L) and in series with a load resistor (R_L) to implement the oscillation neuron. Figure 5a shows the measured oscillation waveforms of the neuron at different input pulse voltages V_{in} when R_L = 180 kΩ, C_L = 200 nF, where continuous oscillation signals are detected. An enlarged

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Table 2. Comparison of Various Ag-Based TS Diffusive Memristors

material system	V_{th}, V	V_{hold}, V	V_{th}, C_V	V_{hold}, C_V	selectivity	I_{cc}, μA	I_{leak}, pA	endurance cycle	ref
Pt/HfO_2/Ag	0.567	0.200	31%	32%					35
Pt/HfO_2/Ag-NDs	0.588	0.271	4.8%	6.9%	$>10^8$	100	<1	$>10^8$	35
Pt/TiO_2/Ag	0.240	0.150	13.5%	14.2%	$\sim10^7$	10	<10		51
Pt/Ta_2O_5/Ag	0.35	0.12			$\sim10^7$	10	<10		52
Pt/Ta_2O_5/np-Pt/Ag	0.383	0.217	4.2%	16.6%	$>10^7$	10	<1	$>10^6$	this work

version of the oscillation waveforms is shown in Figure S8. The oscillation frequencies were derived using fast Fourier transformation (FFT) of the oscillation current. From the FFT plots (Figure S9), the derived oscillation frequencies were 51, 97, 146, and 195 Hz for V_{in} = 0.5, 0.6, 0.7, and 0.8 V, respectively. The oscillation frequency increased as a function of the pulse amplitude of V_{in}, as described in eq 1, where the oscillation frequency is inversely proportional to the RC time constant and logarithmically dependent on V_{in}. As V_{in} increases, the term $\ln\left(\frac{V_{hold}-V_{in}}{V_{th}-V_{in}}\right)$ decreases, indicating a reduction in the charging and discharging times of the load capacitor. Consequently, the frequency of the oscillation increases. By fitting the oscillation frequency to this function, the RC time constant, τ, can be extracted, which is consistent with the behavior of an RC model shown in Figure 5b. This self-oscillation behavior arises from recursive switching between the high-resistance state (R_{OFF}) and the low-resistance state (R_{ON}), driven by the voltage-dependent formation, rupture, and reformation of conductive filaments. Below V_{th}, the device remains in R_{OFF}, while surpassing V_{th} induces a transition to R_{ON}, allowing current to flow. The device reverts to R_{OFF} when the voltage drops below V_{hold}, resulting in periodic switching and self-oscillation. These results indicate that the 10 nm np-Pt TS device exhibits self-oscillation behavior, enabling precise weight sensing of the RRAM synapse when connected to a neural network array.[7] Our novel device configuration suggests that the incorporation of np-Pt significantly improved the switching characteristics of the diffusive memristor by modulating the formation and stability of the conductive filament, leading to enhanced switching uniformity and reduced variability. Table 2 summarizes the various Ag-based switching characteristics of the device.

4. CONCLUSIONS

In conclusion, the resistive switching characteristics of Ag-based threshold switching (TS) memristors with a nanoporous-Pt (np-Pt) cation limiter have been investigated. Incorporating a 10 nm np-Pt layer between Ag and Ta_2O_5 has resulted in significant enhancements in device performance, including high selectivity ($>10^7$), ultralow leakage current (<1 pA), narrower V_{th}/V_{hold} distribution, high endurance ($>10^6$ cycles), and ultra-steep switching slope (~0.01 mV/dec). These improvements are attributed to the electrochemical interactions between Ag and Pt, coupled with the limited cation injection across the dielectric matrix by the np-Pt layer. Furthermore, a comparative analysis using a 20 nm np-Pt cation limiter underscores the importance of optimizing the np-Pt thickness to achieve an improved threshold switching performance. A systematic study of the oscillation characteristics reveals that the oscillation frequency increases with the input voltage. The realization of artificial neurons with low operational voltage variations via the np-Pt cation limiter presents a viable strategy for creating more robust memristive artificial neural networks.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.4c01900.

Surface morphology of different thicknesses of np-Pt thin film, cross-sectional TEM analysis, $I-V$ hysteresis curves for different np-Pt thicknesses at different compliance current levels, V_{th} and V_{hold} cycle-to-cycle statistical distribution (negative voltage region) for 10 nm np-Pt device, V_{th} cycle-to-cycle cumulative probability plot for different thicknesses of np-Pt, device-to-device boxplot comparison for no np-Pt and 10 nm np-Pt devices, switching slopes at different compliance current levels for 10 nm np-Pt device, enlarged analysis of oscillation waveforms, and FFT analysis of TS oscillatory neuron (PDF)

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Notes

The authors declare no competing financial interest.

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