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Programmable Spin–Orbit-Torque Logic Device with Integrated Bipolar Bias Field for Chirality Control

*Gerard Joseph Lim, Daniel Chua, Weiliang Gan, Chandrasekhar Murapaka, and Wen Siang Lew**

Driven by the need to address both the von Neumann bottleneck and scaling limits predicted by Moore's law, spintronic devices have been shown to be strong contenders for logic-in-memory applications. While several field-free spin–orbit torque (SOT)-driven logic devices have been proposed, their operation typically requires additional initialization or reset pulses, the exchange-coupled canted spins reduce both anomalous Hall sign-to-noise ratio as well as thermal stability of the ferromagnetic layer, and device-to-device variation in exchange coupling strength is expected. A reconfigurable SOT-driven logic device using a double Hall cross structure with an integrated bias field line for the generation of a local bias field is experimentally demonstrated. The on-chip bipolar bias field can be toggled to flip the SOT-induced switching chirality, and to assist with deterministic SOT magnetization switching, thereby enabling on-the-fly reconfigurability of the logic device to function as one of the several possible logic gates, e.g., AND, NOR, XNOR, XOR, NIMP, and converse NIMP. It is then shown through compact-modeling and circuit simulation that the applications of such reconfigurable logic devices can be further expanded to build half-adders.

1. Introduction

The spin degree of freedom has enabled the development of nonvolatile, high-speed, ultralow energy dissipation, and scalable spin-based sensors and memory devices. These devices utilize the spin property of the electron rather than relying on electronic charge alone as a state variable, and address device level issues such as high dynamic and standby power dissipation due to leakage current, and heat dissipation inherent to conventional silicon-based complementary metal-oxide-semiconductor (CMOS) technology.[1] The spin-transfer torque Magnetic Random Access Memory (STT-MRAM) is one of the successful and commercially available spintronic products. Its inherent nonvolatility, relatively high speed, low power dissipation, as well as quasi-infinite endurance make it an attractive alternative to transistor-based devices.[2,3] As STT-MRAM devices scale progressively, read disturbance becomes a critical barrier to overcome.[4,5] More recently, highly efficient current-induced switching techniques have been achieved in spin-based devices with large spin–orbit coupling (SOC) materials such as heavy metals (HM) Ta and Pt, allowing write and read current paths to be decoupled.[6–8] By injecting an in-plane electrical current through a HM, spin polarized electrons accumulate at the interface of the HM/ferromagnet (FM). The transverse spin current exerts torque on the magnetization of the FM layer, leading to deterministic spin–orbit torque (SOT) switching. For devices with perpendicular magnetic anisotropy (PMA), the polarity of a symmetry-breaking in-plane field parallel to the direction of current flow determines the chirality of SOT switching.[9,10] In many cases, it is advantageous to eliminate the use of external magnetic fields. As such, field-free magnetization switching has been demonstrated by FM or antiferromagnetic (AFM) coupling.[11,12]

Apart from memory units, spin-based devices also show potential in logic-in-memory applications.[13–20] In this paper, we experimentally demonstrate a stateful SOT logic device, with a balanced ternary output that can be further processed to represent conventional Boolean logic outputs. The Boolean logic outputs due to the logical inputs can be reconfigured by changing the device magnetization and/or the read current scheme. We further demonstrate current-induced magnetization switching (CIMS) with an integrated bias field line for the generation of a local Oersted field, effecting only the intended device and sparing adjacent devices from an external field otherwise provided by an electromagnet. This design allows for on-the-fly reconfigurability by the switching chirality, and does not require initialization or reset current pulses that increase write latency.[16,21,22] The proposed SOT-driven logic device can both store and process data, and would serve as a promising reconfigurable spin–orbit torque driven nonvolatile logic-in-memory device.

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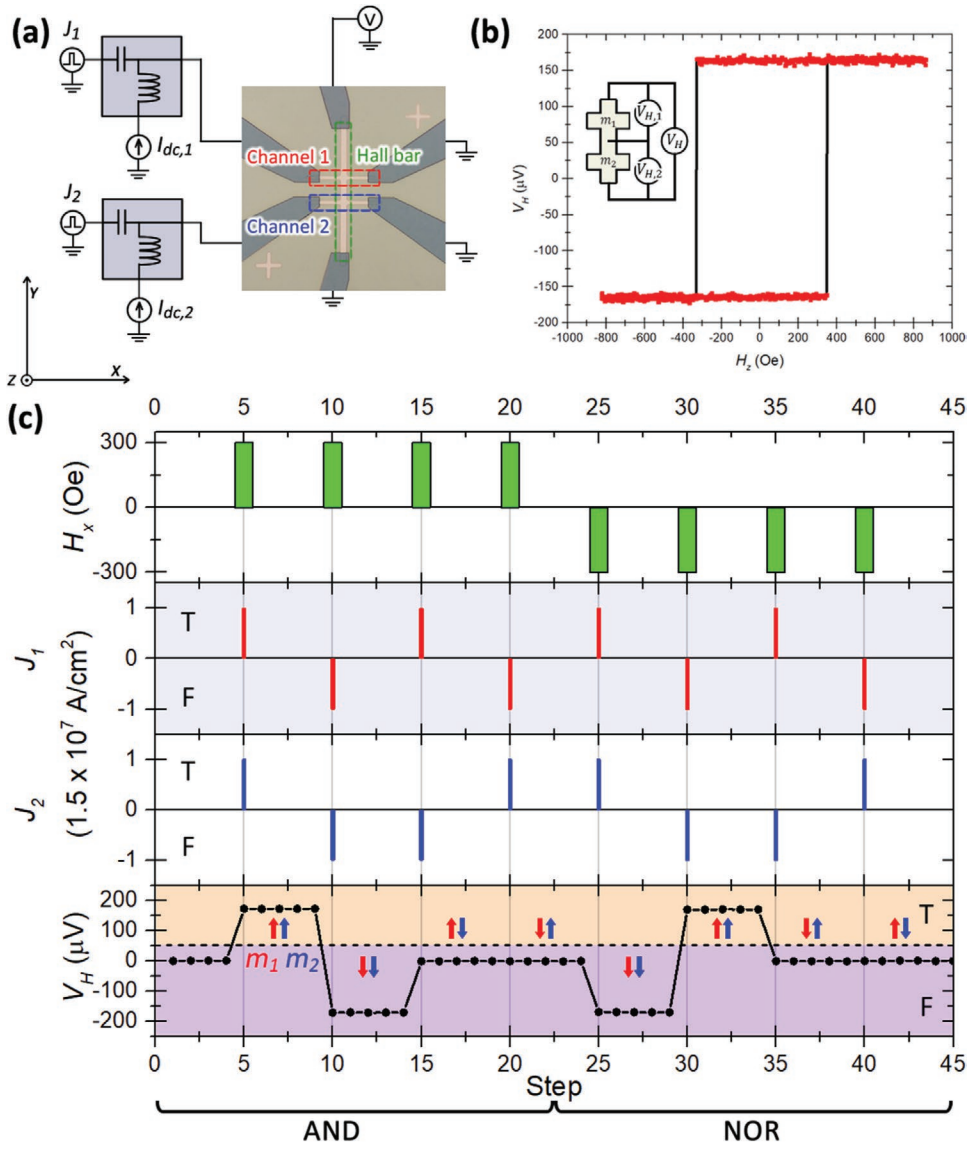


Figure 1. Schematic and operation of the spin–orbit torque driven logic device. a) Device structure and measurement setup. A bias tee enables write pulse and probing currents through each channel. Hall voltage is probed along a common Hall bar. b) Cumulative anomalous Hall voltage V_H in a sweeping out-of-plane magnetic field H_z. The sharp transitions at about $|H_c| = 350$ Oe indicate that the magnetization at each channel have about the same switching field H_c. c) Experimental verification of AND and NOR logic operations based on device output for the same sequence of write input parameters at $H_x = 300$ Oe followed by $H_x = -300$ Oe.

2. Results and Discussions

Perpendicularly magnetized thin films of Ta/Pt/[Co/Pt]$_3$/Co/Ta were deposited on thermally oxidized Si substrates by dc magnetron sputtering at a base pressure better than 5×10^{-8} Torr. Numbers in parentheses indicate nominal film thicknesses in nanometers and the subscript indicates the number of [Co/Pt] bilayer repeats. The device structure was patterned using electron beam lithography and Ar ion milling techniques, resembling two identical Hall crosses sharing one common Hall bar. The double Hall cross structure is henceforth singularly referred to as a "logic device." The wire widths were 5 μm, and electrical contacts comprising Ti (5)/Cu (100)/Ta (5) were patterned and deposited at the wire ends. Channels 1 and 2 as well as the common Hall bar are identified in red, blue, and green dashed boxes, respectively (**Figure 1**). A bias tee enables write $J_n = 1.5 \times 10^7$ A cm^{-2} and read $I_{dc,n} = 100$ μA currents to be delivered through each channel n, and the cumulative anomalous Hall voltage $V_H = V_{H,1} + V_{H,2}$ can be probed along the Hall bar. Since $V_H \propto I_{dc} m_z$, V_H provides an indication of the magnetization of the device.

To ensure that the PMA is preserved in the patterned logic device, V_H was probed in a scanning OOP field H_z as shown in Figure 1b. The resulting hysteresis loop shows sharp transitions at $|H_c| = 350$ Oe, from which can be inferred that the magnetization at the channel junctions switch at about the same H_c. As the junctions are of similar geometry and multilayer structure, it can be assumed that $|V_{H,1}| \approx |V_{H,2}|$.

For magnetization switching to take place in spin-transfer torque (STT) driven devices such as STT-MRAM, a fixed layer provides the necessary spin polarization of an otherwise unpolarized charge current. The spin polarized current then passes through a free layer where momentum exchange results in magnetization rotation and switching. On the contrary, such fixed layer is unnecessary for SOT-driven magnetization switching. An unpolarized charge current flowing through a HM layer with large SOC results in spin accumulation at the interfaces, which diffuses into an adjacent ferromagnetic layer and applies a torque to the magnetization, leading to magnetization switching. For SOT to induce deterministic switching in devices with PMA, the magnetization must be canted toward the $\pm x$-direction orthogonal to both the anisotropy axis ($\hat{z}$) and spin polarization ($\hat{y}$).[9] This can been achieved with an externally applied field H_x,[10] or via exchange coupling with an adjacent magnetic layer.[12] The former allows for improved anomalous Hall signal-to-noise ratio as the magnetization canting can be toggled on and off, as well as reconfigurability by switching the magnetic field direction to achieve polymorphic logic device functionality. On the other hand, the latter affords an integrated solution for magnetization canting. As such, a means of localizing the required magnetic field using an integrated bias field line will afford us the advantages mentioned. SOT-driven switching was achieved using 100 ns write pulses of current density J_1, $J_2 = \pm 1.5 \times 10^7$ A cm^{-2} in the presence of H_x. After each write process, the magnetization state of the device was determined by measuring V_H with a probing current $I_{dc,n} = \pm 100$ μA concurrently through each channel n. The current-induced SOT switching curve shows deterministic magnetization switching for individual Hall crosses (Section S1, Supporting Information).

2.1. Modes of Operation

As there are two sets of input information that can be varied—the magnetization states and the read currents—we can describe the logic device to operate in two different modes as described in **Table 1**. In each mode of operation, the logic gate is a fixed parameter that defines the function of the logic device, such as AND, XOR, or NOR gates, while the logical inputs vary between "true" and "false" permutations—TT, TF, FT, FF.

In mode I, the device logic gate functionality is determined by $I_{dc,n}$ and the magnetization states m_1 and m_2 can be varied. We demonstrate the logic functionality of the device by performing current-driven SOT magnetization switching in the presence of an externally applied field $H_x = \pm 300$ Oe provided by an electromagnet. In subsequent discussions, we vary J_n rather than m_n. By assuming a positive θ_{SH} in our device multilayer stack, the outcome of the magnetization state at each channel junction is summarized as

$$J_n \cdot H_x > 0 \Rightarrow +m_{z,n}$$

$$J_n \cdot H_x < 0 \Rightarrow -m_{z,n}$$

The logical inputs for the device are represented by Boolean "true" (T) or "false" (F), corresponding to $\pm J_n = \pm 1.5 \times 10^7$ A cm^{-2} through each channel n. Figure 1c shows V_H output due to logical inputs TT, FF, TF, and FT for both polarities of H_x. The dashed line in the V_H output plot indicates a threshold that can be used to interpret the ternary output of V_H = (−200, 0, +200) μV as a Boolean output by half rectification, represented by orange and purple regions.

For H_x = +300 Oe, logical inputs of TT and FF result in V_H = +200 μV and −200 μV, respectively, while both TF and FT result in $V_H \approx 0$ μV. This results in the truth table for logical AND. For H_x = −300 Oe, the V_H output for each combination of logical inputs are negated, and we recover the truth table of a NOR gate. As previously mentioned, the cumulative V_H is due to the anomalous Hall voltages formed across each channel junction. Due to the identical junction geometry and multilayer structure, as well as the same write and probe current amplitudes that result in the same magnetization states m_1 and m_2 set at each junction, $|V_{H,1}| \approx |V_{H,2}|$. In mode I, the persistent device magnetization states can be switched, and the outputs can be recovered by probing the logic devices using the same read scheme. However, it may not be energy-efficient to operate the device by repeatedly changing magnetization states.

Writing device magnetization states repeatedly is energy expensive. In mode II, the device magnetization is the fixed quantity, and the read scheme can act as the logical inputs. After writing the device magnetization state once, different outputs can be achieved by varying the logical read inputs. The in situ differential Kerr images (MagVision Kerr microscopy system) show the four different logic device magnetization configurations—a) Up-Up, b) Up-Down, c) Down-Up, and d) Down-Down—where dark(light) contrasts correspond to up(down) states at each junction (**Figure 2**). The devices used for Kerr microscopy images had channels placed more closely for imaging purposes, while actual devices used in measurements had channels spaced approximately 20 μm apart to minimize current shunting (Section S2, Supporting Information). For each configuration, the probing inputs permutate between TT, TF, FT, and FF, where T and F corresponds to $+I_{dc,n}$ and $-I_{dc,n}$, respectively. Further processing to half-rectify ($V_H > 0$) or full-rectify ($|V_H|$) the outputs can be implemented to expand the range of logic to include NOR, XNOT, AND, XOR, NIMP, and converse NIMP. The outputs for mode II are also summarized in the table for all four permutations of the logic device magnetization states.

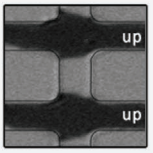
Table 1. Operating modes of logic device. Modes I and II are defined by the varying magnetization states or write schemes, respectively.

	Mode I	Mode II
Logic Gate (fixed parameter)	Fixed read scheme $I_{dc,1}$ and $I_{dc,2}$	Fixed magnetization states m_1 and m_2
Logical Inputs (varying parameter)	Varying magnetization states m_1 and m_2	Varying read scheme $I_{dc,1}$ and $I_{dc,2}$

2.2. On-the-Fly Reconfigurability by Bias Field Line

A method for localizing the necessary H_x to achieve deterministic switching with switching chirality control would

a)



Up-Up

$I_{dc,1}$	$I_{dc,2}$	V_H	Half Rectification	Full Rectification
T	T	+200μV	T	T
T	F	0	F	F
F	T	0	F	F
F	F	-200μV	F	T
			AND	XNOR

b)

Up-Down

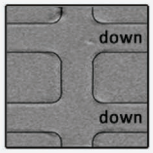
$I_{dc,1}$	$I_{dc,2}$	V_H	Half Rectification	Full Rectification
T	T	0	F	F
T	F	+200μV	T	T
F	T	-200μV	F	T
F	F	0	F	F
			NIMP	XOR

c)

Down-Up

$I_{dc,1}$	$I_{dc,2}$	V_H	Half Rectification	Full Rectification
T	T	0	F	F
T	F	-200μV	F	T
F	T	+200μV	T	T
F	F	0	F	F
			Converse NIMP	XOR

d)



Down-Down

$I_{dc,1}$	$I_{dc,2}$	V_H	Half Rectification	Full Rectification
T	T	-200μV	F	T
T	F	0	F	F
F	T	0	F	F
F	F	+200μV	T	T
			NOR	XNOR

Figure 2. Kerr microscopy images of a single logic device at logic device magnetic states a) up-up, b) up-down, c) down-up, and d) down-down, with corresponding truth table. Outline of the logic device is for visual distinction from substrate. Interpretation of the logic device for different read schemes using half- or full-rectification.

allow for selectively manipulating individual logic devices. In our approach, a bias field line that is electrically isolated from the device by a dielectric can generate a large enough Oersted field for magnetization switching, omitting the need for an externally applied field. In our experiment, the dielectric used was 200 nm of HfO_2 sputtered over a rectangular region, sufficient for electrically isolating the device from the subsequent patterning and deposition of a bias field line comprising Ti (5)/Cu (150)/Ta (5). The bias field line was fabricated such that the Oersted field generated along the device channels would be coaxial to J, and the field is not capable of switching the perpendicularly magnetized states independently. The direction and amplitude of the Oersted field can be tuned by simply changing the magnitude and polarity of the current I_{FL} running through it. This offers an on-chip solution to field generation that is local to each device, allowing for reconfigurability without perturbing neighboring devices. The resultant device has polymorphic logic functionality. **Figure 3** shows the optical microscopy image of the logic device with the integrated bias field line separated from the device by a passivation layer of HfO_2. The cross-section A-A along the length of one of the channels is shown in Figure 3b. By changing the polarity of I_{FL}, the Oersted field along the device channels can be switched between $+\hat{x}$ and $-\hat{x}$ directions.

We demonstrate the logic functionality of the logic device with the integrated bias field line. First, 30 mA is applied through the bias field line. Then, write current pulses of $J = \pm 1.5 \times 10^7$ A cm^{-2} is delivered through each channel in the four possible permutations. The current flowing through I_{FL} is turned off after the write procedure, and I_{dc} = 100 μA is delivered through the channels to probe the magnetization state of the logic device between each set of write current pulses. The additional energy expense for the bias field generation for each write operation is estimated to be under 1 nJ for a 10 Ω field line of equivalent 100 ns pulse. Figure 3c shows V_H for corresponding inputs of I_{FL}, J_1, and J_2. In our device, the magnetization state does not require initialization.

The device shows similar behavior as achieved with an externally applied magnetic field, and the bias field line provides the same necessary magnetic field for magnetization canting with the added advantage of allowing individual device programming (Section S3, Supporting Information).

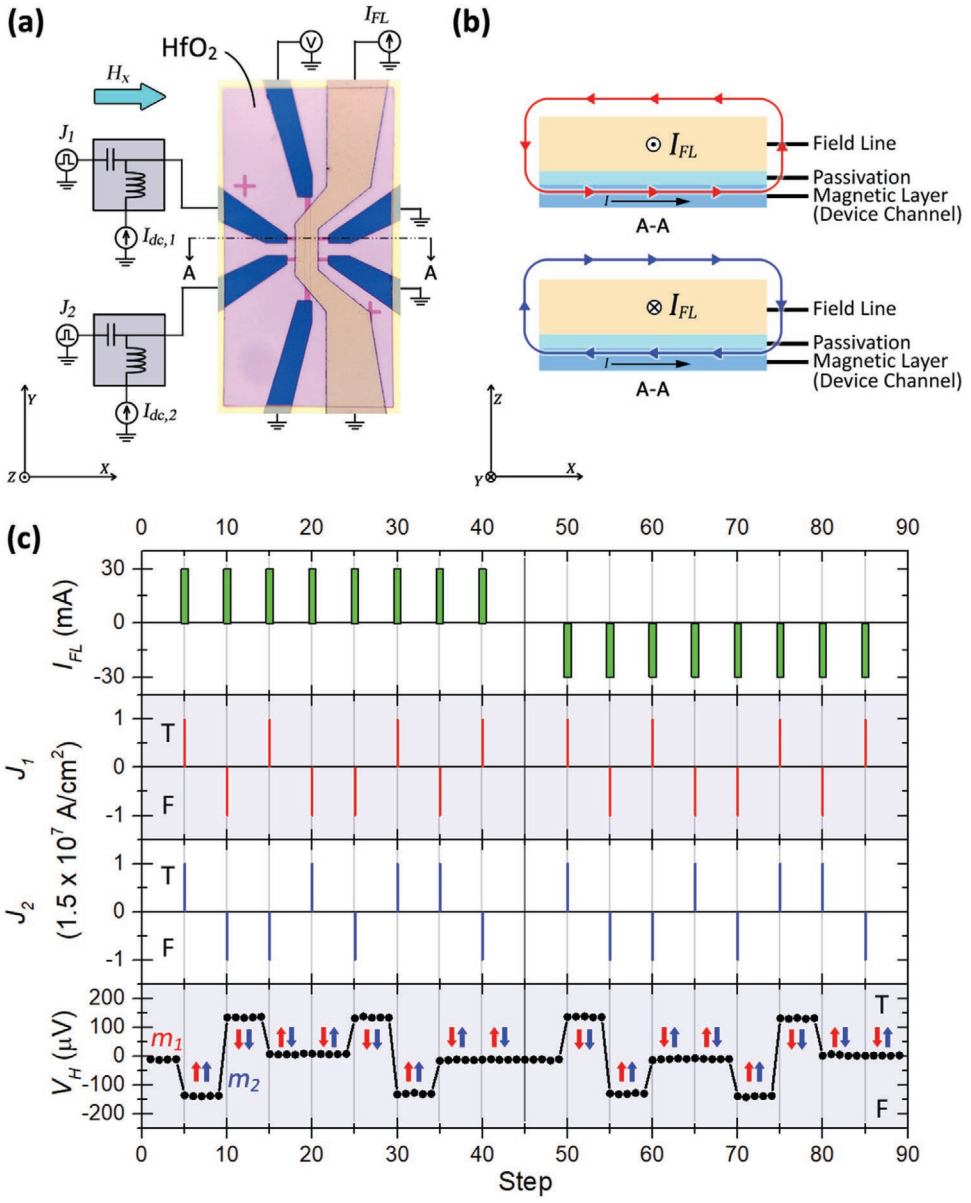


Figure 3. Schematic diagram overlaid on optical microscopy image of the spin–orbit torque driven logic device with integrated bias field line. a) The device structure and measurement setup. b) Illustration of local Oersted field generation due to current along the bias field line. c) Experimental verification of device output for the same series of write input parameters at $I_{FL} = 30$ mA and $I_{FL} = -30$ mA.

2.3. Compact Model of a Reconfigurable Spin Orbit Torque Logic Device

We now demonstrate a half-adder by constructing a SPICE-compatible compact model of our device. The compact model was realized using the modular approach pioneered by Camsari et. al.[23] In this formalism, different spintronic phenomena are represented by elemental circuit modules, which can then be combined to model device behavior.

Three pieces of device physics are necessary for the modelling of each of the multilayer Hall cross device: i) charge to spin conversion by the spin Hall effect (SHE), ii) magnetization dynamics governed by the Landau–Lifshitz–Gilbert (LLG) equation and iii) magnetization state readout by the anomalous Hall effect (AHE). The circuit models of these three phenomena are shown in **Figure 4**. The SHE circuit model was developed by Hong et. al.,[24] and is equivalent to solving the charge and spin diffusion equations together with the generalized Ohm's law used to quantify spin Hall phenomena.[25] The circuit model consists of a charge circuit which models the motion of charge current in the longitudinal direction and a spin circuit which models the motion of spin current in the transverse direction. The two circuits are coupled by current sources, which represent conversion between charge and spin currents via the SHE and the inverse spin Hall effect (ISHE).

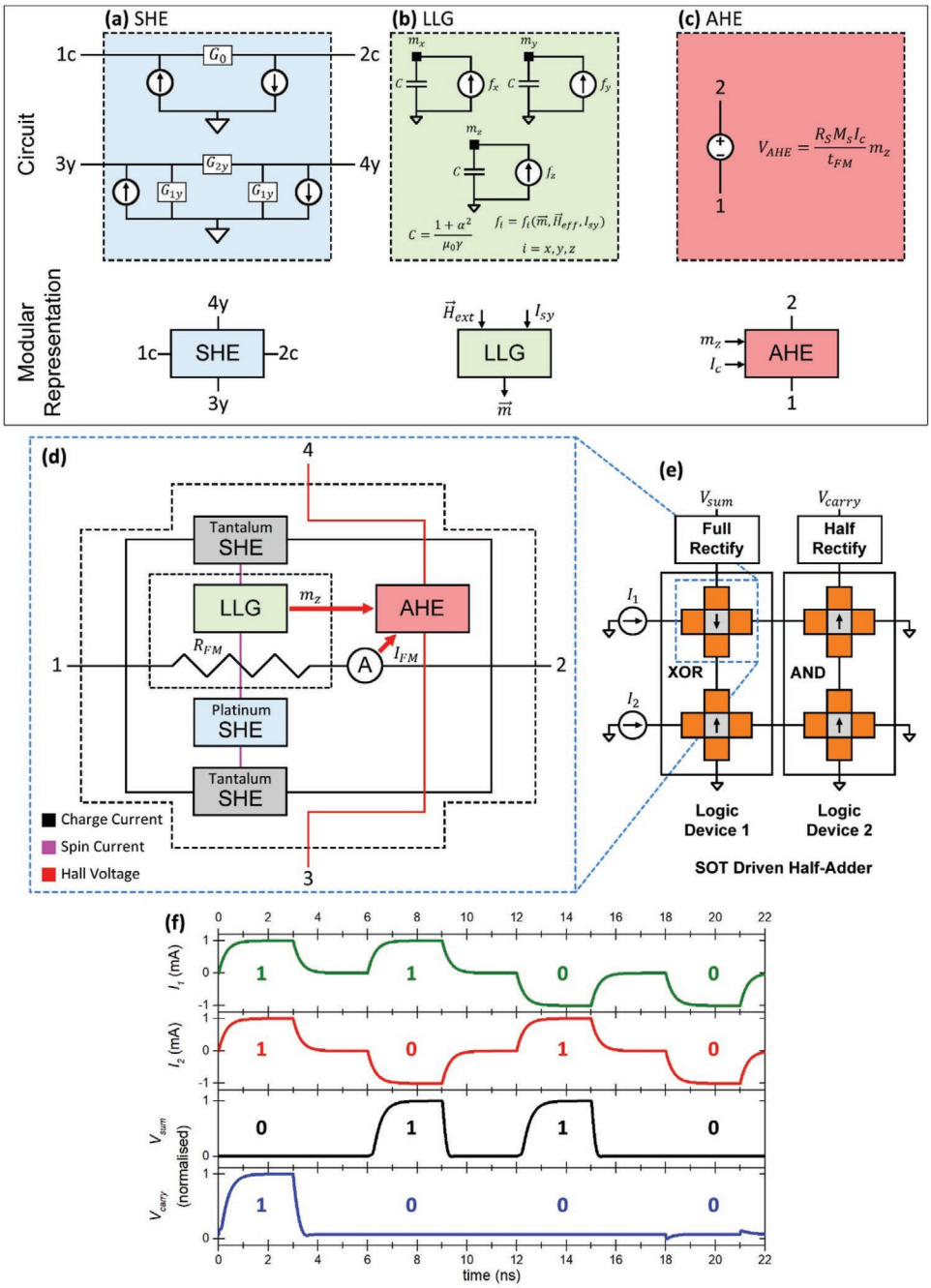


Figure 4. SPICE-compatible compact model of logic device and functional application as half-adder. a) The SHE circuit is represented by coupled charge and spin circuits.[24] The charge circuit between terminals 1c and 2c contains a series conductance G_0 and two current sources I_{0c} which represent spin-to-charge conversion via the inverse spin Hall effect (ISHE). The spin circuit between terminals 3y and 4y consists of a series conductance G_{2y}, shunt conductances G_{1y} which represent spin current attenuation via spin–flip processes, and current sources I_{0y} which represent charge to spin conversion by the SHE. b) Capacitor–current source circuits which represent the LLG equation. Magnetization components m_x, m_y, and m_z are represented as node voltages. c) Voltage source circuit representation of the AHE where $V_{AHE} \propto I_c M_z$. Modular representations of the SHE, LLG, and AHE are shown under their respective circuit representations.[23] d) Compact model of our multilayer Hall cross device. The HM layers are modelled using SHE modules while the FM layer is modelled using an LLG module and resistance R_{FM}. The AHE module accepts m_z from the LLG module and the current flowing through the FM layer I_c as inputs and outputs a transverse voltage V_{AHE}. The correlation between the compact model to the symbolic representation is shown in blue dashed lines. Black arrows represent the magnetization state of the Hall cross, where an ↑ indicates $m_z > 0$ and ↓ indicates $m_z < 0$. e) Design of half-adder circuit using two logic devices. Devices 1 and 2 have magnetization configurations and rectification circuits that yield the logical outputs of an XOR and AND gate respectively. Current sources are wired to the devices such that input current pulses can be delivered to both devices simultaneously. f) Demonstration of half-adder functionality.

The LLG equation used in this work is as follows

$$\frac{d\vec{m}}{dt} = -\gamma\mu_0\vec{m}\times\vec{H}_{\text{eff}} + \alpha\vec{m}\times\frac{d\vec{m}}{dt} + \frac{\gamma\hbar}{2eM_sV}\vec{m}\times(\vec{m}\times I_{sy}\hat{y}) \quad (1)$$

where $\vec{m}$ is the unit magnetization, $\vec{H}_{\text{eff}}$ is the effective field which consists of external field and uniaxial anisotropy field terms, α is the Gilbert damping coefficient, γ is the gyromagnetic ratio, M_s is the saturation magnetization of the FM layer and V is its volume. The vector triple product on the right-hand side is the damping-like (DL) torque caused by an incident pure spin current of magnitude I_{sy} and polarization $\hat{y}$. The corresponding circuit model in Figure 4b consists of capacitor–current source circuits where the node voltage corresponds to the components of $\vec{m}$. Our implementation is based on the one presented by Bonhomme et. al.,[26] and can reproduce the dynamics of a single domain ferromagnet in accordance with Equation (1). A similar implementation can be found in reference.[27]

The AHE is represented by a voltage source as shown in Figure 1c. The anomalous Hall voltage generated due to small read current I_c is given by the following formula

$$V_{AHE} = \frac{R_sM_sI_c}{t_{FM}}m_z \quad (2)$$

where R_s is the anomalous Hall coefficient,[28] M_s is the saturation magnetization of the FM layer, and t_{FM} is its thickness (Section S4, Supporting Information). As $V_{AHE} \propto m_zI_c$, the transverse voltage generated by the AHE will have a polarity determined by the sign of m_z for a given read current I_c. This allows for the simulation of magnetization state read-out within a circuit simulator. The derivation of Equation (2) is given in Section S4 in the Supporting Information.

The SHE module accepts charge current inputs through its 1c and 2c terminals and outputs y-polarized spin current through its 3y and 4y terminals. The LLG module accepts spin current I_{sy} and the external field $\vec{H}_{\text{ext}}$ as inputs, and outputs the unit magnetization $\vec{m}$. The AHE module accepts m_z and the charge current flowing through the FM layer as inputs and outputs the transverse voltage V_{AHE} according to Equation (2).

The three modules are used to construct a compact model of our Hall cross device as shown in Figure 2a. Parameters used are shown in Section S5 in the Supporting Information. Recall that our device consists of the Ta (5)/Pt (3)/[Co (0.6)/Pt (0.6)]$_3$/Co (0.6)/Ta (5) multilayer stack: The Ta and Pt layers are modelled using SHE modules. The [Co/Pt]$_3$/Co multilayer is approximated as a bulk FM layer with perpendicular anisotropy, and modelled using the LLG module with charge current resistance R_{FM}. The SHE modules and R_{FM} are connected in parallel to approximate the current flow through the HM and FM layers. Upon passing a charge current between terminals 1 and 2, the HM layers generate a spin current which is then fed to the LLG module via the spin current line. An external field $\vec{H}_{\text{ext}}$ can also be specified and passed to the LLG module as an input. The LLG module would then calculate the trajectory $\vec{m}(t)$. The z-component of the magnetization m_z as well as the charge current flowing through the FM layer I_{FM} would then be inputs to the AHE module. It would then generate a transverse voltage V_{AHE} using Equation (2), which can be measured using nodes 3 and 4. The compact model schematic in Figure 4d can be treated as a subcircuit with four nodes, representing a single Hall cross in which charge current can be passed between nodes 1 and 2. This charge current can be used to write magnetization states via torque resulting from SHE or to sense magnetization states by measuring the voltage due to AHE across nodes 3 and 4.

A half-adder circuit can be constructed as shown in Figure 4e. The circuit consists of two logic devices. Each logic device is modelled by two Hall crosses (upper and lower) with their AHE voltage sources arranged in series with each other. A half adder consists of a XOR and an AND gate defined by the magnetization states of each logic device in accordance with operating mode II. The two logic devices are connected in series, such that current inputs I_1 and I_2 are concurrently delivered across the upper and lower Hall crosses of each logic device, respectively. In this arrangement, the logical inputs to both devices are read current pulses and the logical outputs are rectified AHE voltages. The XOR and AND gates generate the SUM and CARRY outputs, respectively. In order to obtain the correct logic functionality, the two devices must be set to the correct magnetization configurations. Logic device 1 is initialized with its upper Hall cross in the "down" ($m_z < 0$) state and its lower Hall cross in the "up" ($m_z > 0$) state. The total transverse AHE voltage generated by logic device 1 would then undergo amplification and full-wave rectification in order to obtain the correct logical output. Similarly, logic device 2 is initialized with both Hall crosses in the up state and its total transverse AHE voltage would undergo amplification and half-wave rectification.

We now demonstrate the half-adder functionality by cycling through the four possible logical input combinations. In Figure 4f, logical inputs are delivered by I_1 and I_2 as exponential pulses with 3 ns pulse widths and 1 mA pulse amplitudes. The positive pulses are interpreted as logical 1s and the negative pulses are interpreted as logical 0s. The SUM and CARRY outputs are shown as black and blue voltage waveforms in Figure 4f. The output voltages close to zero are interpreted as logical 0 and the positive voltages are interpreted as logical 1. Hence, we have shown that the circuit in Figure 4e functions as a half-adder. Our logic device can be used as elements in larger systems with other applications. Also, as each device can be reconfigured by magnetization switching, the design shown in Figure 4e can be made more flexible by adding a suitable multiplexer between the Hall cross devices and the rectification circuits. Such a design could expand the functionality of the circuit shown in Figure 4e and allow for greater flexibility during operation.

3. Conclusion

We have demonstrated a reconfigurable spin–orbit torque driven logic device. The logic device performs similarly with an external magnetic field generated by an electromagnet, as it would with a local Oersted field by an integrated bias field line for each logic device, demonstrating the viability of locally controlling the parameters for magnetization switching for each device. The device has also shown to logically output AND, NOR, XNOR, XOR, NIMP, and converse NIMP, using either of two modes. The first mode being write- and energy-intensive, and is useful

for applications requiring the encoding of data for long term memory storage. The second mode is more energy-conservative, where the device states that determine the logic gate function are written once. Mode II is demonstrated in a SPICE-compatible compact modelling of the logic in a half-adder application. Spintronic-based computation by SOT switching as demonstrated in this work has the potential to lead to low power and high speed spintronic circuits logic and computation.

4. Experimental Section

Ta (5)/Pt (3)/[Co (0.6)/Pt (0.6)]$_3$/Co (0.6)/Ta (5) (thickness in nanometer) was deposited on thermally oxidized Si substrates by dc magnetron sputtering at a base pressure better than 5×10^{-8} Torr at room temperature. The subscript indicates the number of [Co/Pt] bilayer repeats. The thin film stack is perpendicularly magnetized as-deposited. The blanket films were patterned using electron beam lithography and Ar ion milling techniques, resembling two identical Hall crosses sharing one common Hall bar. The wire widths were 5 µm, and electrical contacts comprising Ti (5)/Cu (100)/Ta (5) were patterned and deposited at the wire ends. After fabrication, the devices were measured using 4-terminal Hall voltage measurement using a Keithley 2400. An external magnetic field was provided by a LakeShore EM4 electromagnet. For integrated bias field operation, the device was situated away from external magnetic field sources. For logic operation, a bias tee was used to couple the probing dc input from a Keithley 2400 with the RF input from a Picosecond Pulse Labs 10,300B. Current through the bias field line was provided by a second unit of Keithley 2400.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

Boolean logic, reconfigurable logic devices, spin logic, spin–orbit torque, threshold logic

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