Nanomagnetics

Programmable Logic Operation via Domain Wall Profile Manipulation

Han Kheng Teoh*, Sarjoosing Goolaup**, and Wen Siang Lew***

School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371
** Student Member, IEEE*
*** Member, IEEE*
**** Senior Member, IEEE*

Received 13 Apr 2015, revised 7 May 2015, accepted 12 May 2015, published 18 May 2015, current version 16 Jun 2015.

Abstract—In this paper, we propose a prototype domain wall (DW) programmable magnetic logic device that is able to perform the AND and OR logic functions. The device operates by manipulating the information encoded in the internal spin structure of a transverse domain wall (TDW). The input and output bits in this scheme are the transverse profiles of the domain wall. By exploiting the inherent pinning and depinning mechanisms of the TDW within the device structure, the output DW profile can be deterministically controlled. The logical operation can be programmed at run time by the application of a local Oersted field.

Index Terms—Nanomagnetics, domain wall dynamics, domain wall logic, magnetic logic.

I. INTRODUCTION

Conventional microelectronic-integrated circuits work by controlling the flow of electrons through transistor switches. Power consumption and scaling limitations in conventional semiconductor electronics are driving developments of alternative logic technologies. Spintronics, which exploits the electron spin, offers the promise of devices that outstrip the performance of traditional semiconductor electronics. Magnetic logic architecture takes advantage of the spin degree of freedom of electron to enable low energy consumption and high-speed nonvolatile devices [Wolf 2001].

The manipulation of the binary state of nanomagnets via external magnetic field or spin transfer torque effect has spawned numerous techniques for magnetic logic [Allwood 2002, Imre 2006, Xu 2008, Franken 2012]. Domain wall in magnetic nanowires has attracted a great deal of interest as a potential candidate for both memory and logic device applications [Allwood 2005, Parkin 2008]. In such proposals, magnetization reversal is controlled within a region on a patterned nanostrip, which in turn yields ordered segmentations of magnetic orientation that are used for data representation.

In thin narrow nanowires, transverse domain walls (TDWs) are the stable configurations. TDWs can be categorized as head-to-head DW or tail-to-tail DW, depending on which direction the magnetic moments are oriented. A further degree of freedom associated with the TDW is the chirality of the transverse component. For logic operations, information can be encoded and processed in the internal states of magnetic domain wall. This concept enables mobile data bit within the system. We have previously shown experimentally the logic NOT operation based on DW profile manipulation [Goolaup 2015]. In this paper, we extend the domain wall profile logic to two-bit operations and introduce a device that is programmable at runtime. This device is capable of performing logical AND or OR operations via a current controlled gate. The operation of the device is via the differential speed of TDW reaching the junction. The inherent spin orientation within the device selectively delays the motion of incoming DW.

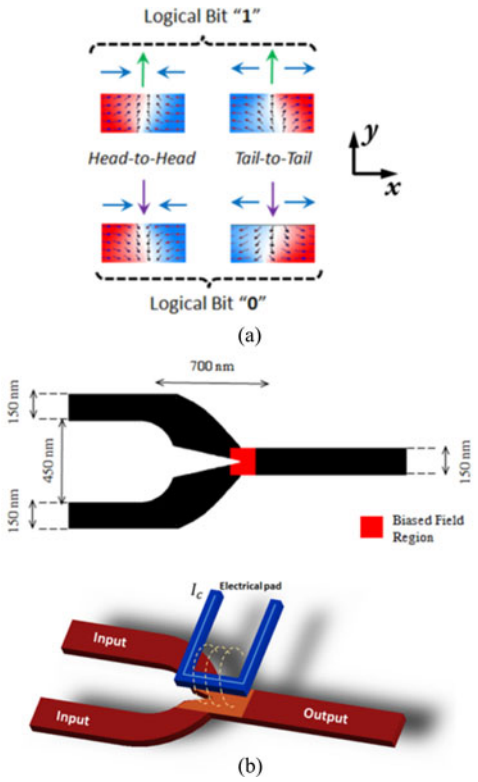


Fig. 1. (a) Logical bit representation, with transverse magnetization pointing "up" assigned as logical "1" and transverse magnetization pointing "down" assigned as logical "0," for both head-to-head and tail-to-tail domain walls. (b) Schematic representation of magnetic structure with two input branches and one output branch. An electrical pad is patterned atop the junction to allow for programmable operation.

The bit representation for the proposed logic scheme is depicted in Fig. 1(a). The bits "0" and "1" correspond to the transverse profile pointing in the $-y$ (down profile) and $+y$ (up profile)-orientations, respectively. In our structure, irrespective of the

Corresponding author: W. S. Lew (wensiang@ntu.edu.sg). H. K. Teoh and S. Goolaup contributed equally to this work.
Digital Object Identifier 10.1109/LMAG.2015.2434801

type (head-to-head or tail-to-tail) of TDW, the device structure allows for repeatable logical operation via control of the DW transverse profile.

A schematic of the device structure is shown in Fig. 1(b). The device comprises two input nanowires that are tapered to merge into a single output nanowire. The logical operation is carried out within the tapered segment of the device. For proper device operation, the opening angle at the junction has to be between 5° and 25°. A metallic pad is placed atop the junction between the inputs and output. By flowing current through the metallic pad, a local Oersted field can be generated at the junction. The Oersted field acts as a gate to select the type of logical operation to be carried out by the device. For device clocking, an external pulsed magnetic field can be applied along the nanowire axis (*x*-axis).

To ensure that TDW is stable within the device structure, the width and thickness of the nanowire have to obey the relationship

$$t_{\text{crit}} w_{\text{crit}} \leq 130A/\mu_0 M_s^2 \tag{1}$$

where t is film thickness, w is the width of the nanowire, A and M_s are the exchange constant and saturation magnetization of the ferromagnetic material, respectively, and μ_0 is the permeability of free space [McMichael 1997]. In our device structure, we have chosen the nanowire width to be 150 nm, ferromagnetic material $Ni_{80}Fe_{20}$, and a film thickness of 5 nm. The distance between the two input nanowires has to be greater than twice the width of each input nanowire so that any interaction between the two input DWs can be minimized. In this particular device, the spacing between the two input nanowires was 450 nm.

II. MODELING DOMAIN WALL DYNAMICS

Micromagnetic simulations were carried out using object-oriented micromagnetic framework (OOMMF) code from the National Institute of Standards and Technology [Donahue 1999]. The parameters used in the simulations for $Ni_{80}Fe_{20}$ were: saturation magnetization $M_s = 860 \times 10^3$ A/m, exchange constant $A = 1.3 \times 10^{-11}$ J/m, anisotropy constant $K = 0$, and a damping constant $\alpha = 0.5$. A unit cell size of $5 \times 5 \times 5$ nm^3 was used in all the simulations. For all simulations, a fixed external field of 25 mT was applied along the *x*-axis.

The DW dynamics and resulting DW in the output nanowire are presented in Fig. 2. The spin state evolution within the structure when both input TDWs have the transverse profile along the $+y$ (up profile)-orientation is depicted in Fig. 2(a). In the initial state, the magnetic spins within the tapered region follow the geometrical contour of the device structure. As such, within the tapered region, spins pointing toward the upper input nanowire adopt a relative $+y$-orientation, while spins pointing toward the lower input nanowire adopts a relative $-y$-orientation.

The input TDW in the upper nanowire has an "up" profile that is in the same direction as the spin profile at the tapered region. As such, the TDW merges with the spins at the tapered region. For the DW propagating through the lower nanowire, the transverse profile of the DW and the spins in the tapered region are in the opposite direction. This leads to the TDW being pinned at the entrance of the tapered region as seen in Fig. 2(a)-ii.

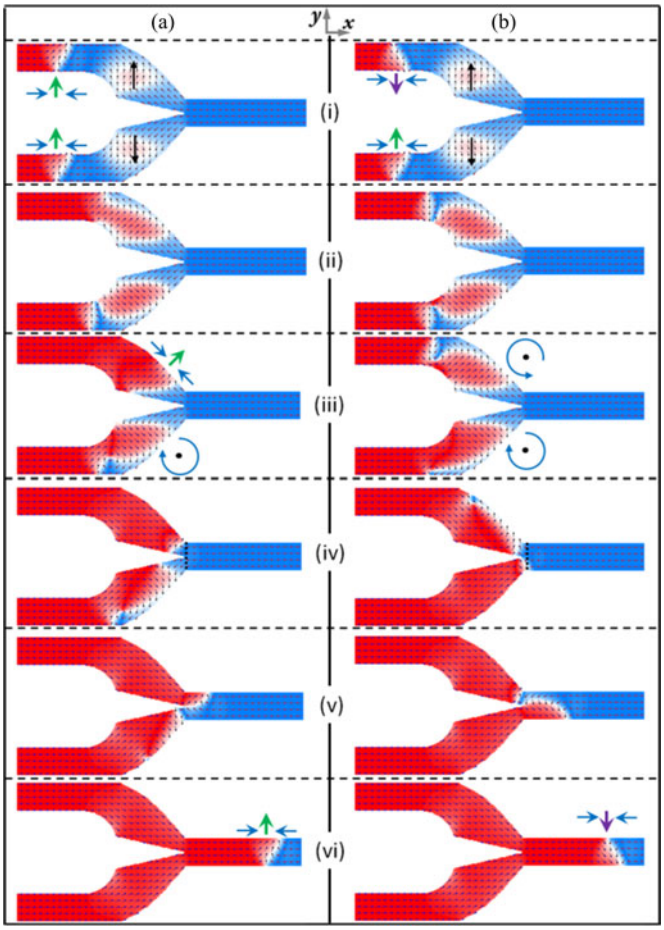


Fig. 2. Simulated head-to-head domain wall dynamics with a fixed external field of 25 mT and no field bias at the junction. (a) Domain wall with "up" profile in each input branch. (b) Domain wall with "down" profile in upper branch and "up" profile in lower branch.

The spin profile from the upper segment of the tapered region is pushed toward the junction. At the lower segment, the TDW transforms into a vortex DW (Fig. 2(a)-iii). The motion of the vortex core in the lower branch pushes the $-y$ spins within the tapered region toward the junction. Due to the intrinsic pinning and subsequent nucleation and annihilation of the vortex DW, the spins from the lower region reach the junction slightly later as compared to the spins from the upper segment. Our simulation results show that the time difference between the two profiles reaching the junction is $\Delta t \approx 1.5$ ns. The spin configuration that reaches the junction first, propagates within the output nanowire, and eventually stabilizes as a TDW with spins in the $+y$-orientation. Following this operation, the spin configurations within the structure are primed for the next logical operation. This ensures that there is no need to reset the device after every logic operation.

As the output DW profile expands throughout the width of the output nanowire, the "up" DW profile propagates from the upper to the lower edge of the junction. The "up" DW profile moves into the junction toward the pinned DW profile at the lower region. The interaction between the "up" and "down" DW leads to the annihilation of the "down" DW profile.

Similarly, when the two input TDWs have their profile along the $-y$ (down)-orientation, the output DW has a profile along the

$-y$ (down)-orientation. This is because the TDW in the upper nanowire is now pinned at the entrance of the tapered region and has to undergo DW transformation. This implies that when the two input TDWs are identical, the output TDW has the same profile as the input.

Fig. 2(b) depicts the spin evolution when the two input TDWs have opposite profiles. In this particular configuration, the TDW profile in the upper nanowire has a "down" orientation, while the lower nanowire has an "up" orientation. As both TDWs have opposite profiles as compared to their respective tapered segment, they undergo pinning and transformation into vortex configurations as depicted in Fig. 2(b)-iii. This in turn pushes the profile of the tapered region toward the junction, leading to the profile from the upper and lower segment to reach the junction simultaneously. In this instance, the profile from the lower branch reaches the junction first. The time difference between the two profiles reaching the junction was $\sim$0.5 ns. The profile from the lower segment propagates through the output nanowire and results in an output TDW with a "down" profile. Further simulations reveal that the output TDW can have either "up" or "down" profile.

When the TDW profile in the upper nanowire is along the $+y$-orientation, and the lower nanowire is in the $-y$-orientation, both TDW undergo similar pinning and depinning mechanisms at their respective tapered segments. The profiles from the tapered segment are pushed to the junction almost simultaneously, with the time difference being in the range of $\sim$0.5 ns. The profile of the output TDW is stochastic similar to the configuration discussed in Fig. 2(b).

In essence, the output TDW of the device structure is determined by which profile within the tapered region reaches the junction first. To enable useful application for the two-input TDW operation, there is a need to deterministically control the output TDW when the TDW dynamics at the lower and upper edge are the same. As our device selects the output based on the profile that reaches the junction first, the speed of the DW (profile) at the junction is a critical parameter. It is known that the speed of a propagating TDW can be affected by the application of field along the nanowire width [Kunz 2008, Bryan 2008].

The effect of a local magnetic field on the motion of a TDW is shown in Fig. 3(a). A field of 10 mT was applied along the y-direction, shaded region along nanowire length, as seen in the inset of Fig. 3(a). When the external field is along the $-y$-orientation, TDW with "down" profile undergoes an increase in speed within the bias region, while TDW with "up" profile is slowed down, as shown in Fig. 3(a)-i. The relative difference in speed is around 80%. The opposite behavior is observed in Fig. 3(a)-ii, when the bias field is applied along the $+y$-orientation. Interestingly, as seen in Fig. 3(a), both head-to-head and tail-to-tail DWs undergo the same speed increase/decrease depending on the chirality.

To achieve a local magnetic field, we make use of a metallic pad atop the junction between the tapered region and the output nanowire. To gain an insight into the Oersted field generated by a current flowing through the metallic pad, COMSOL simulation is used. Shown in Fig. 3(b) are the computed magnetic field direction and strength generated underneath the pad when a current is applied clockwise or anticlockwise through

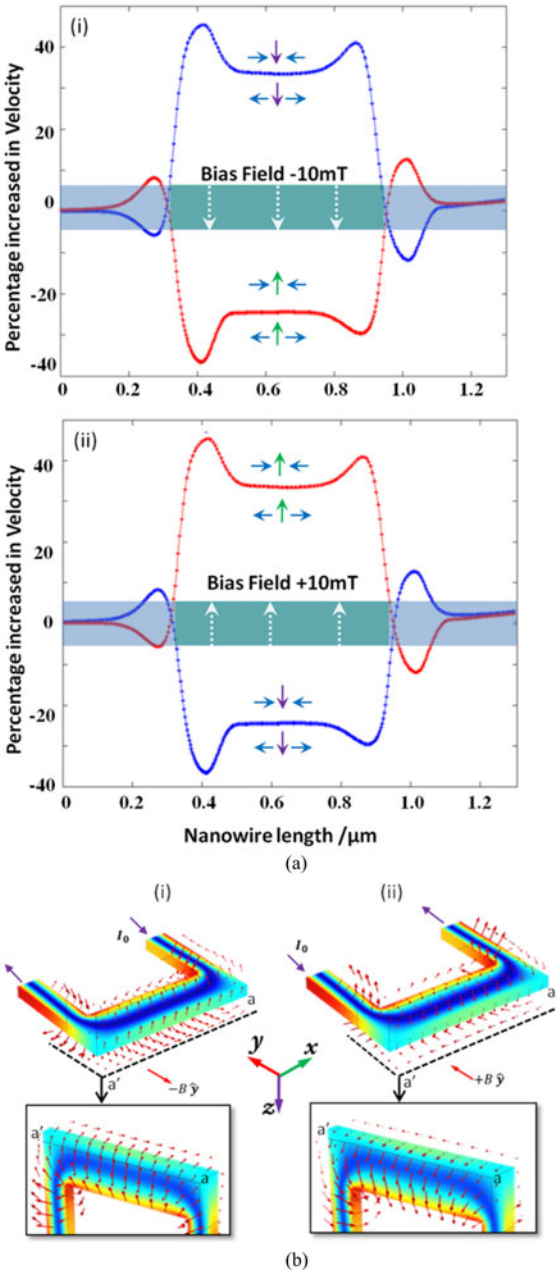
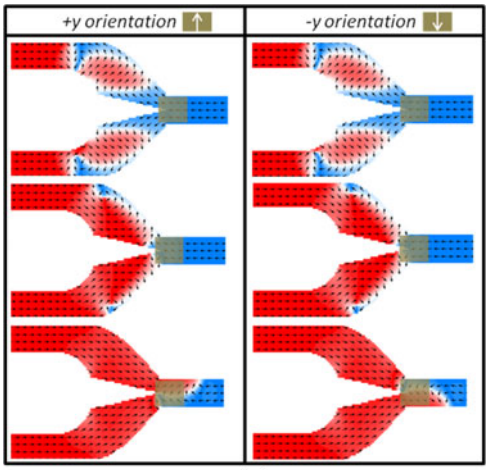


Fig. 3. (a) Domain wall speed under the influence of an external bias field applied transverse to the nanowire length. (i) For fields applied along the $-y$-orientation, the domain wall with "down" profile undergoes an increase in speed while the domain wall with "up" profile is slowed down. (ii) For fields applied along the $+y$-orientation, the domain wall with "up" profile undergoes an increase in speed while the domain wall with "down" profile is slowed down. (b) COMSOL simulation of magnetic field distribution across a metallic strip. (i) For a clockwise current flow, a uniform field along the $-y$-orientation is produced underneath the pad, (ii) while for an anticlockwise current flow, a uniform field along the $+y$-orientation is obtained.

the electrical pad. The arrows indicate the direction of the magnetic field around the pad. As can be seen in Fig. 3(b), a uniform magnetic field along y-orientation can be produced by the metallic pad. A clockwise current orientation gives a magnetic field oriented along the $-y$-direction (Fig. 3(b)-i), while an anticlockwise current results in a field along the $+y$-orientation as seen in Fig. 3(b)-ii.



(a)

Input	Input	Output	
		Bias Field along +y direction	Bias Field along -y direction
↓ {0}	↓ {0}	↓ {0}	↓ {0}
↓ {0}	↑ {1}	↑ {1}	↓ {0}
↑ {1}	↓ {0}	↑ {1}	↓ {0}
↑ {1}	↑ {1}	↑ {1}	↑ {1}
		Logical OR	Logical AND

(b)

Fig. 4. (a) Domain wall evolution in the logic structure under the application of a bias field along the *y*-orientation at the junction, when DWs in both input branches undergo similar pinning processes. For bias field along the $+y$-orientation, the output domain wall has "up" transverse magnetization while for fields along the $-y$-orientation, the output DW has "down" transverse magnetization. (b) Table summarizing the input magnetization configurations and the respective output configurations under the influence of a field bias at the junction.

III. PROGRAMMABLE LOGIC OPERATION

The device operation was simulated by introducing a local bias field of 10 mT along the *y*-direction at the junction. Fig. 4(a) shows the spin state evolution at the junction under the application of a local Oersted field along the *y*-orientation. The input configuration is the same as the one used in Fig. 2(b). The TDW profile in the upper nanowire has "down" orientation, while the lower nanowire has TDW with "up" orientation. Under no local Oersted field, both the DW profiles from the upper and lower tapered region are pushed to the junction simultaneously.

When the local Oersted field is acting along the $+y$-orientation, the DW with "up" profile moves faster underneath the metallic pad. This in turn leads to the output TDW having an "up" profile, as seen in Fig. 4(a). Conversely, when the local bias field is along the $-y$-orientation, the "down" profile is sped up and the output TDW has a "down" profile. The simulations were repeated a number of times and the output TDW always follows the local Oersted field orientation. Our simulation results show that the magnitude of the local bias field underneath the pad can be within the range of 5 to 15 mT.

Interestingly, we note that the bias field has no effect when the TDW undergoes different depinning mechanism within the device, that is, when both input TDWs have the same profile. The table in Fig. 4(b) summarizes the input and output combinations that can be obtained with different gate field bias. We note that for a gate bias with $+y$-field, an OR logical operation is obtained. For a $-y$-field bias, the output exhibits a logical AND operation. This result shows that the type of logical operation can be controlled by the gate at the junction.

IV. CONCLUSION

We have demonstrated the concept of manipulating information using the internal structure of transverse domain wall configurations. The device exploits the domain wall dynamics within a defined structure. By using a local Oersted field as a gate, the operation of the device structure can be programmed at run time. This paves the way for DW-based reconfigurable logic devices. The device is scalable to smaller dimensions. This will result in smaller DW size as well as lower energy to drive the DW.

ACKNOWLEDGMENT

This work was supported in part by the NRF-CRP program (Non-volatile Magnetic Logic and Memory Integrated Circuit Devices) under Grant NRF-CRP9-2011-01 and by the Nanyang Technological University under the Undergraduate Research Experience on Campus (URECA) program.

REFERENCES

Allwood D A, Xiong G, Cooke M D, Faulkner C C, Atkinson D, Vernier N, Cowburn R P (2002), "Submicrometer ferromagnetic NOT gate and shift register," *Science*, vol. 296, pp. 2003–2006, doi: 10.1126/science.1070595.

Allwood D A, Xiong G, Faulkner C C, Atkinson D, Petit D, Cowburn R P (2005), "Magnetic domain-wall logic," *Science*, vol. 309, pp. 1688–1692, doi: 10.1126/science.1108813.

Bryan M T, Schrefl T, Atkinson D, Allwood D A (2008), "Magnetic domain wall propagation in nanowires under transverse magnetic fields," *J. Appl. Phys.*, vol. 103, 073906, doi: 10.1063/1.2887918.

Donahue M J, Porter D G (1999), "OOMMF user's guide, Version 1.0," National Inst. Standards Technol., Gaithersburg, MD, USA, Interagency Report NISTIR 6376.

Franken J H, Swagten H J M, Koopmans B (2012), "Shift registers based on magnetic domain wall ratchets with perpendicular anisotropy," *Nature Nanotechnol.*, vol. 7, pp. 499–503, doi: 10.1038/nnano.2012.111.

Goolaup S, Ramu M, Murapaka C, Lew W S (2015), "Transverse domain wall profile for spin logic applications," *Sci. Rep.*, vol. 5, 9603, doi: 10.1038/srep09603.

Imre A, Csaba G, Ji L, Orlov A, Bernstein G H, Porod W (2006), "Majority logic gate for magnetic quantum-dot cellular automata," *Science*, vol. 311, pp. 205–208, doi: 10.1126/science.1120506.

Kunz A, Reiff S C (2008), "Enhancing domain wall speed in nanowires with transverse magnetic fields," *J. Appl. Phys.*, vol. 103, 07D903, doi: 10.1063/1.2829032.

McMichael R D, Donahue M J (1997), "Head to head domain wall structures in thin magnetic strips," *IEEE Trans. Magn.*, vol. 33, pp. 4167–4169, doi: 10.1109/20.619698.

Parkin S S P, Hayashi M, Thomas L (2008), "Magnetic domain-wall racetrack memory," *Science*, vol. 320, pp. 190–194, doi: 10.1126/science.1145799.

Wolf S A, Awschalom D D, Buhrman R A, Daughton J M, von Molnár S, Roukes M L, Chtchelkanova A Y, Treger D M (2001), "Spintronics: A spin-based electronics vision for the future," *Science*, vol. 294, pp. 1488–1495, doi: 10.1126/science.1065389.

Xu P, Xia K, Gu C, Tang L, Yang H, Li J (2008), "An all-metallic logic gate based on current-driven domain wall motion," *Nature Nanotechnol.*, vol. 3, pp. 97–100, doi: 10.1038/nnano.2008.1.